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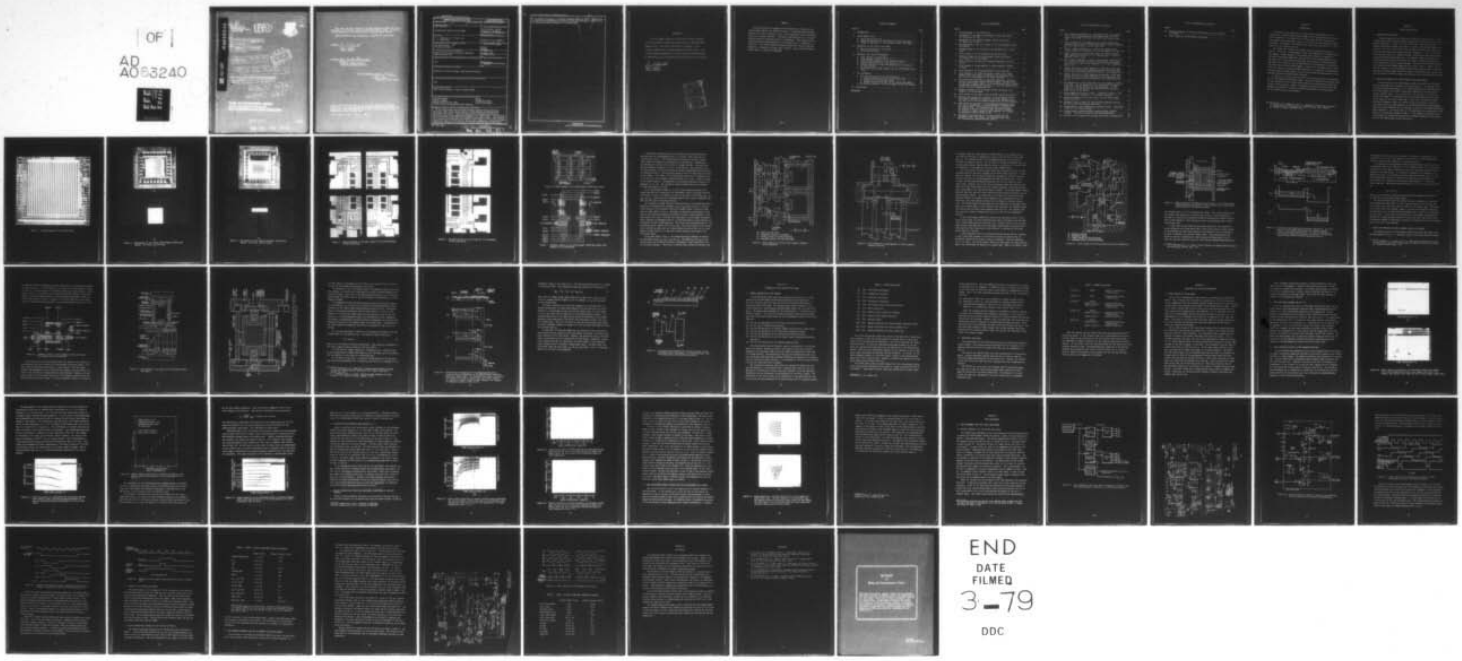

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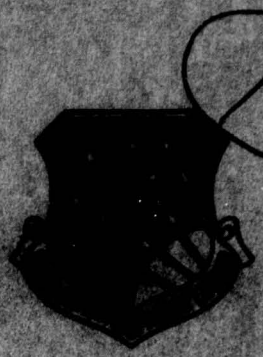

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RCA Laboratories

(10) W. F. Kosonocky, E. G. [redacted]
F. V. Shallcross

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IR-CCD area sensor
IR-CCD line sensor

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The IR-CCD arrays with platinum silicide Schottky-barrier detectors fabricated under this contract contain a 25x50-element area sensor and a 62-element line sensor. The above devices were processed with two-level polysilicon-gate buried-channel CCD registers for image readout. The platinum silicide detectors were made with implanted n-type guard rings. Such construction resulted in sufficiently low detector dark current at 77 K to allow frame-integration times of 30 to 100 ms. The process optimization included high-temperature sintering of the platinum silicide either at 6509 for 10 minutes or

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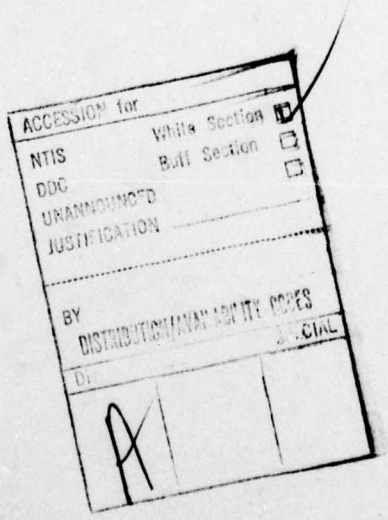
for 30 minutes followed by a 20-minute hydrogen anneal at 550°C. Devices were also made with low-temperature sintering of platinum silicide at 320°C for 8 h in nitrogen followed by another 8 h in forming gas.

EVALUATION

This Final Report describes a half man year effort studying processing parameter changes that would lead to an optimized IRCCD imaging array. The effort concentrated on changing silicide formation temperatures, poly-gate doping, and metallization. The infrared imaging measurements on these devices are being performed at RADC-ESE and will be reported upon the open scientific literature.

Sven A. Roosild

SVEN A. ROOSILD
Project Engineer



PREFACE

This Final Report was prepared by RCA Laboratories, Princeton, New Jersey, under Contract No. F19628-77-C-0172. It describes work performed from April 15, 1977 to March 11, 1978, in the Integrated Circuit Technology Center, J. H. Scott, Director. The project supervisor was D. E. O'Connor and the Principal Investigator was W. F. Kosonocky. Other members of the technical staff who participated in this program were E. S. Kohn and F. V. Shallcross. The IR-CCD devices fabricated during this contract were processed by L. Bijaczyk, R. Miller, and V. Frantz. The Air Force Technical Monitor was S. A. Roosild of RADC/ESE.

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SECTION I

INTRODUCTION

The goal of this program was to study process optimization of two-dimensional, infrared charge-coupled imagers with platinum silicide Schottky-barrier detectors. The masks for the IR-CCD array, TC1199, fabricated in this program, were developed as part of a previous Air Force Contract F19628-73-C-0282. The design of the TC1199 IR-CCD arrays was described in the Final Report [1] for the above contract.

The TC1199 chip contains two IR-CCD arrays with platinum silicide detectors. They are: a 25x50-element IR-CCD area imager and a 62-element IR-CCD line imager. Bonded samples of both imagers were supplied to Deputy for Electronic Technology (RADC/ESE), Hanscom AFB, MA, for thermal-imaging tests. The major part of the device testing under this contract at RCA Laboratories has been probe testing of the processed wafers and room-temperature testing of the bonded line and area IR-CCD imagers. Some of the 62-element IR-CCD imagers were also operated at liquid nitrogen temperature to study the low-temperature transfer losses and dark current as well as the charge-handling capacity of the platinum silicide Schottky-barrier detectors.

In Section II of this report we review the constructions and the operation of the 25x50-element IR-CCD line sensor. Section III describes the process used for the fabrication of the IR-CCD arrays and the processing options exercised as part of this program. Section IV describes the electrical and optical measurements and Section V contains a detailed description of the electronics for the IR-CCD area and line sensors.

---

1. E. S. Kohn, W. F. Kosonocky, and F. V. Shallcross, *Charge-Coupled Scanned IR Imaging Sensors*, Final Report No. RADC-TR-77-308, under Contract No. F19628-73-C-0282, September 1977.

SECTION II

IR-CCD ARRAY TC1199

A. DESCRIPTION OF THE CHIP

A photomicrograph of the IR-CCD chip, TC1199, is shown in Fig. 1. This 230-mil square chip contains two IR-CCD sensors with platinum silicide Schottky-barrier detectors. In Fig. 2 (a) and (b) the front and the back views of a bonded 25x50-element IR-CCD area sensor are shown. The infrared image is projected on this array from the back side through a 190-mil square opening cut in the 28-pin dual-in-line ceramic package. Figures 3 (a) and (b) show the front and back views of a bonded 62-element IR-CCD line sensor with platinum silicide Schottky-barrier detectors. The infrared image is projected onto this array from the back side through the 50-mil x 210-mil opening milled in the 28-pin dual-in-line ceramic package. The IR-CCD area and line sensors are illustrated with higher magnification in Figs. 4 and 5. Figure 4 shows the four corners of the 25x50-element IR-CCD area sensor and Fig. 5 shows the two ends of the 62-element IR-CCD line sensor. The construction and the operation of these two IR-CCD sensors are described in the following two sections.

B. DESIGN AND OPERATION OF 25x50-ELEMENT IR-CCD AREA SENSOR

A block diagram of the 25x50-element IR-CCD area sensor with platinum silicide Schottky-barrier detectors is shown in Fig. 6. This sensor has an interline-transfer organization. The infrared detectors are separated from the buried-channel CCD (B-CCD) column shift register by vertical surface-channel transfer gates. In the staring mode of operation of this device, the detected image is transferred from the infrared detectors to the B-CCD column registers once every frame time. Then, while the detectors start a new frame integration time, the original frame is transferred a line at a time from the B-CCD column registers to the B-CCD horizontal output register, from which each horizontal line is read out in series by the floating-diffusion output amplifier. The construction of this area sensor is illustrated in more detail in the schematic diagram in Fig. 7. This diagram illustrates all of the elements and identifies the electrical terminals required for the operation of the 25x50-element IR-CCD area sensor.

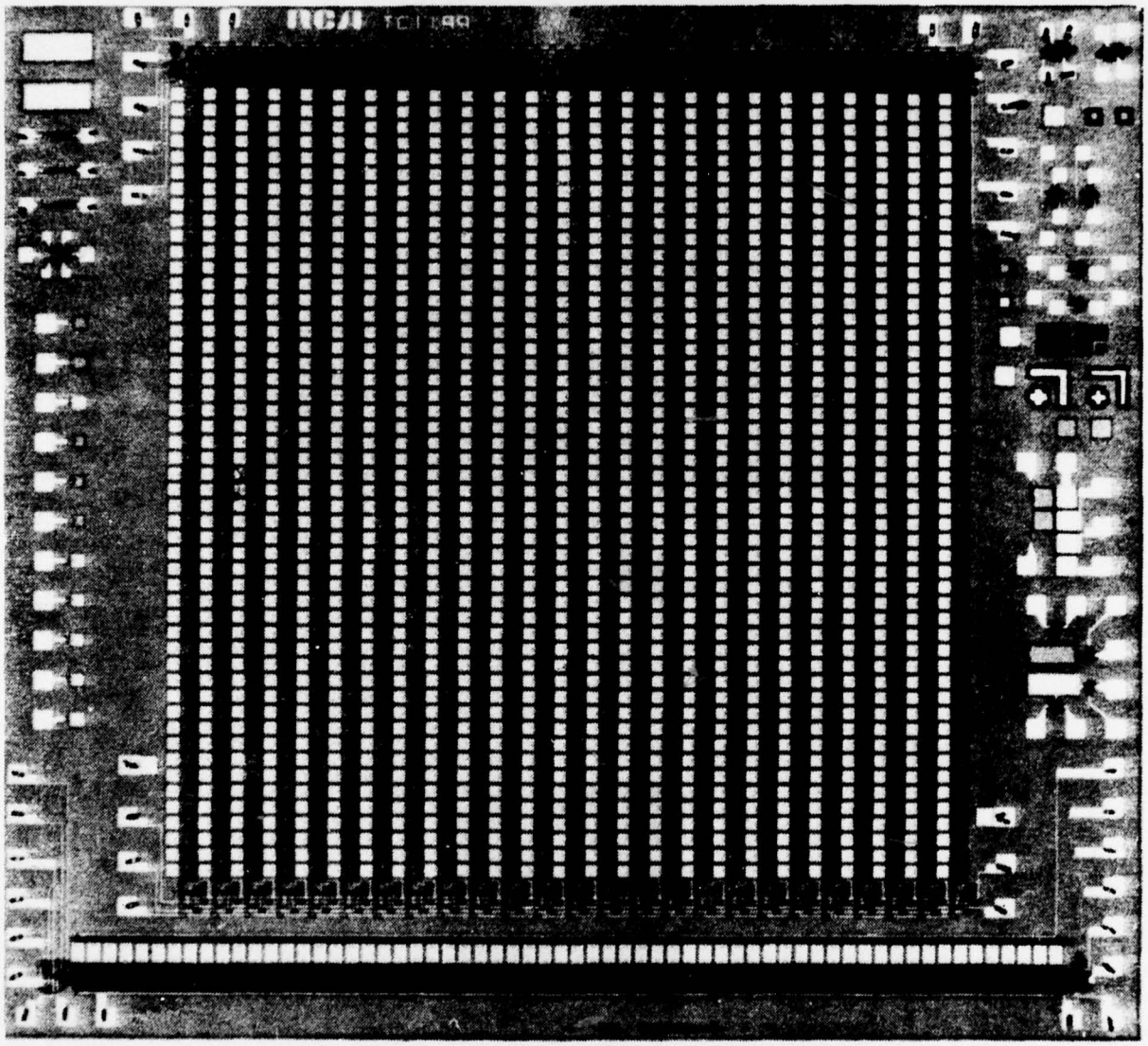
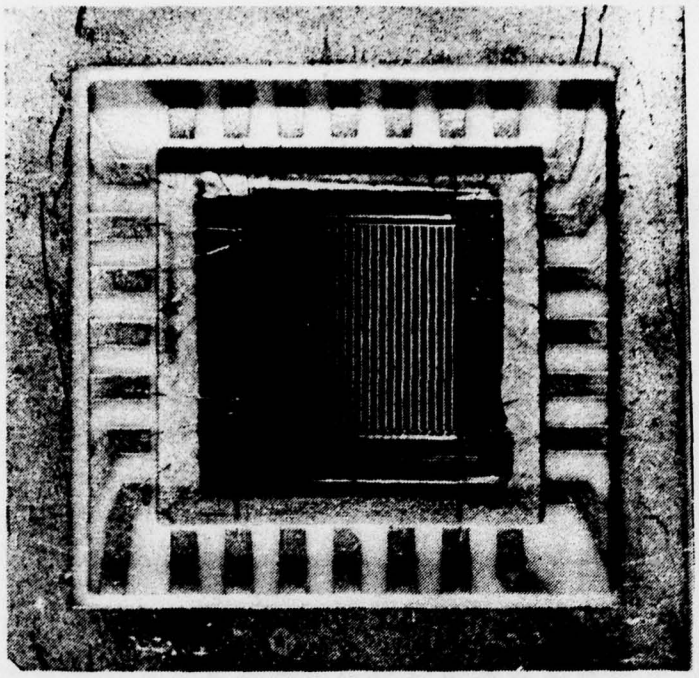


Figure 1. Photomicrograph of the TC1199 chip.



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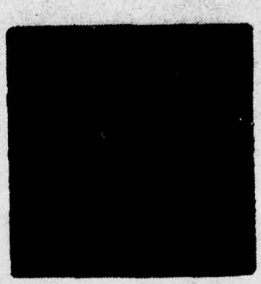
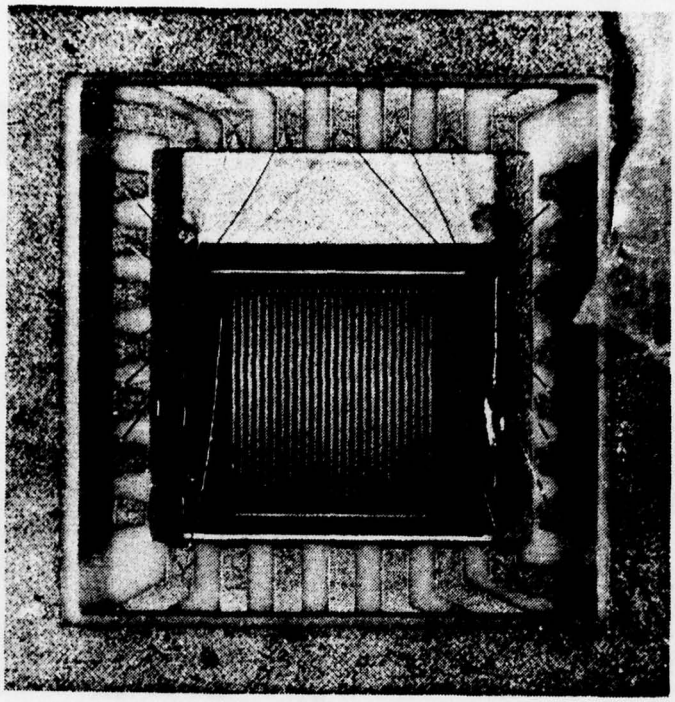
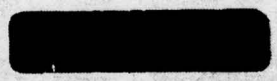


(b)

Figure 2. Photographs of the bonded 25x50-element IR-CCD area sensor: (a) front, and (b) back.



(a)



(b)

Figure 3. Photographs of the bonded 62-element IR-CCD line sensor: (a) front, and (b) back.

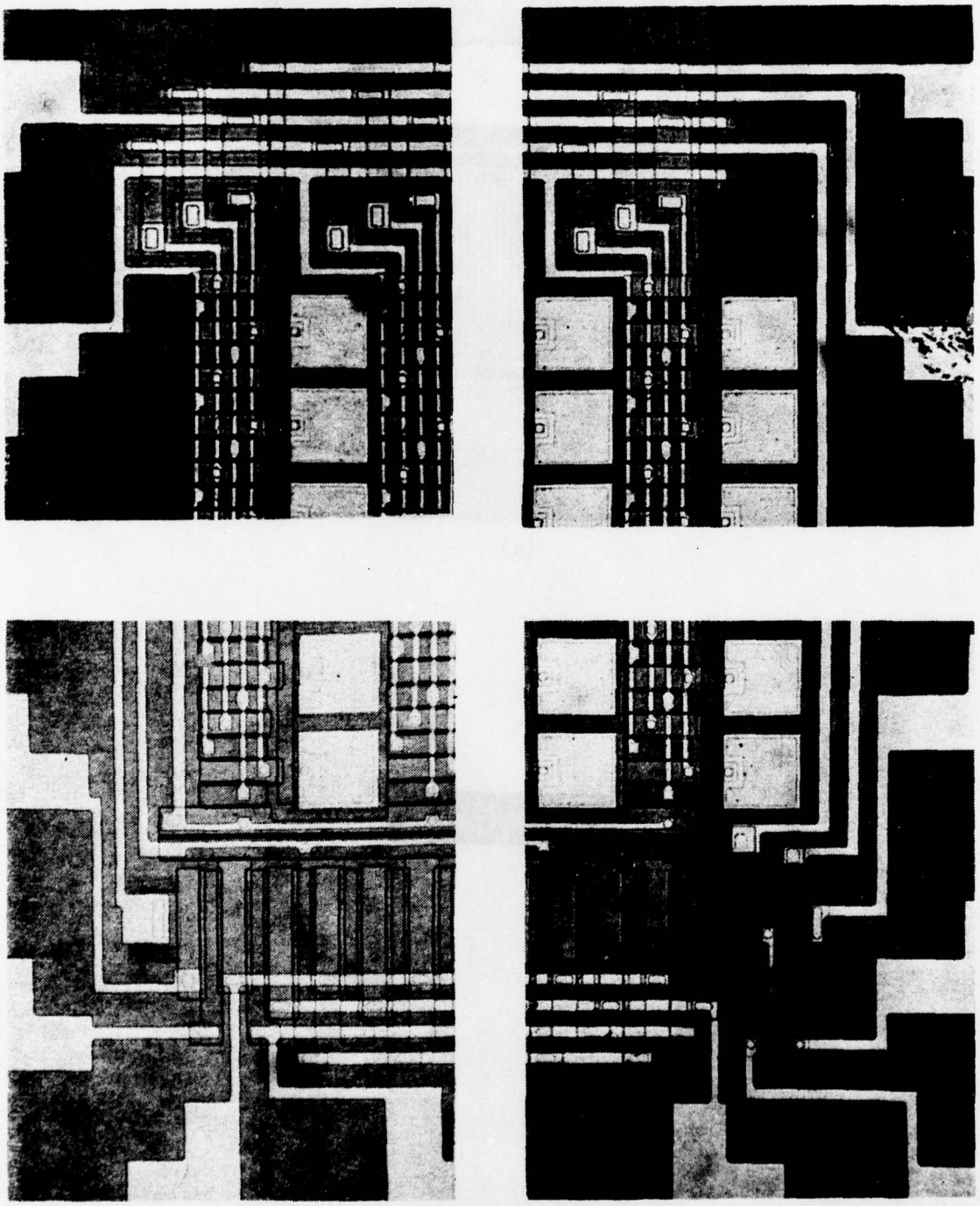


Figure 4. Photomicrograph of the four corners of the 25x50-element IR-CCD area sensor.

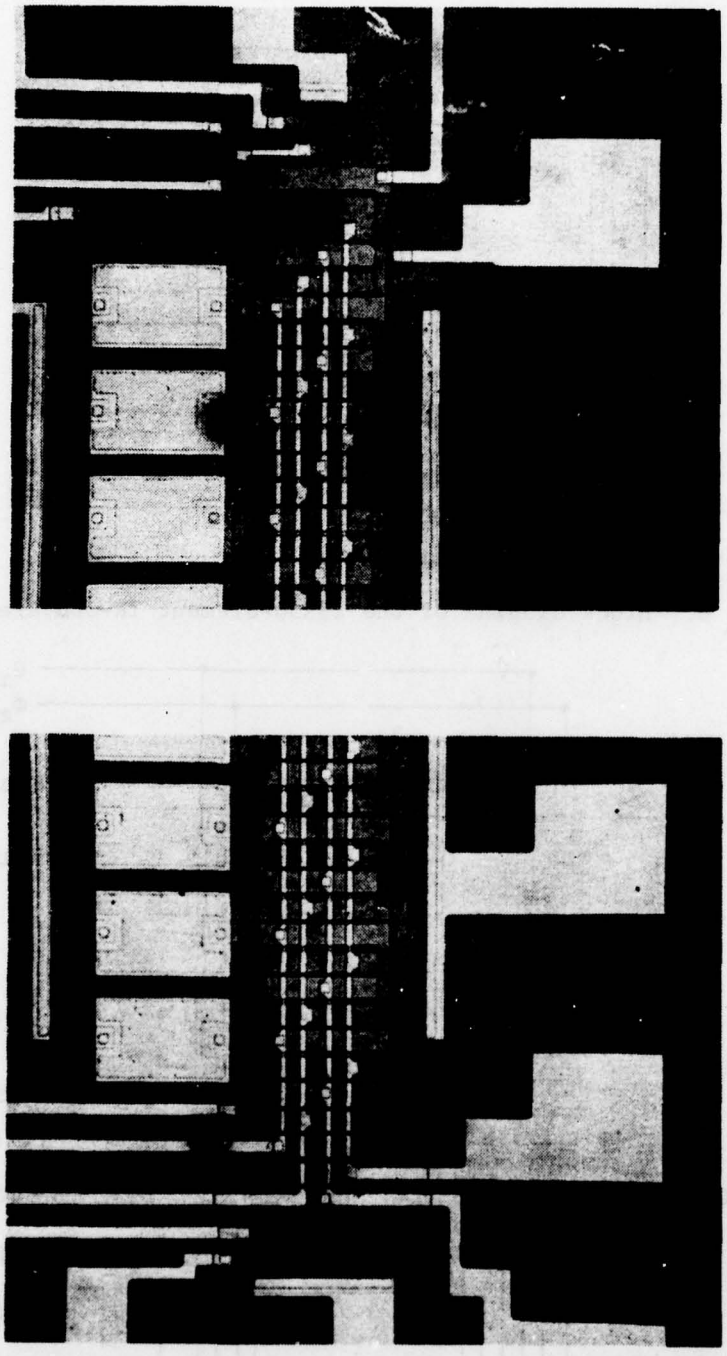


Figure 5. Photomicrograph of the two ends of the 62-element IR-CCD area sensor.

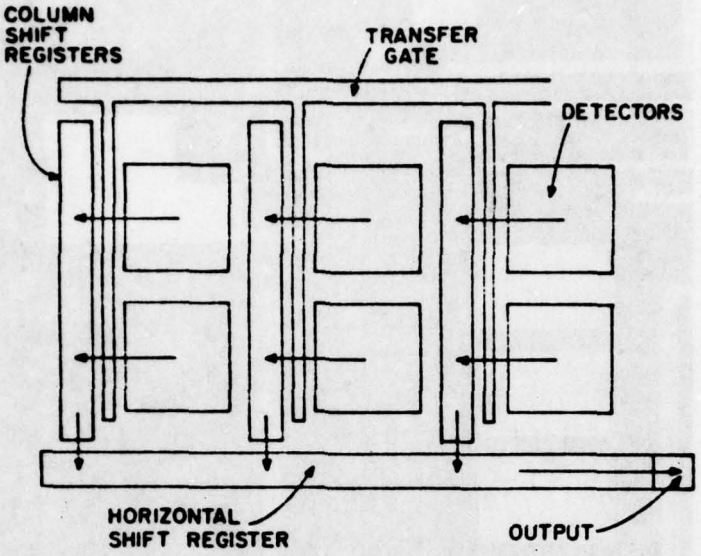


Figure 6. Block diagram of the 25x50-element IR-CCD area sensor.

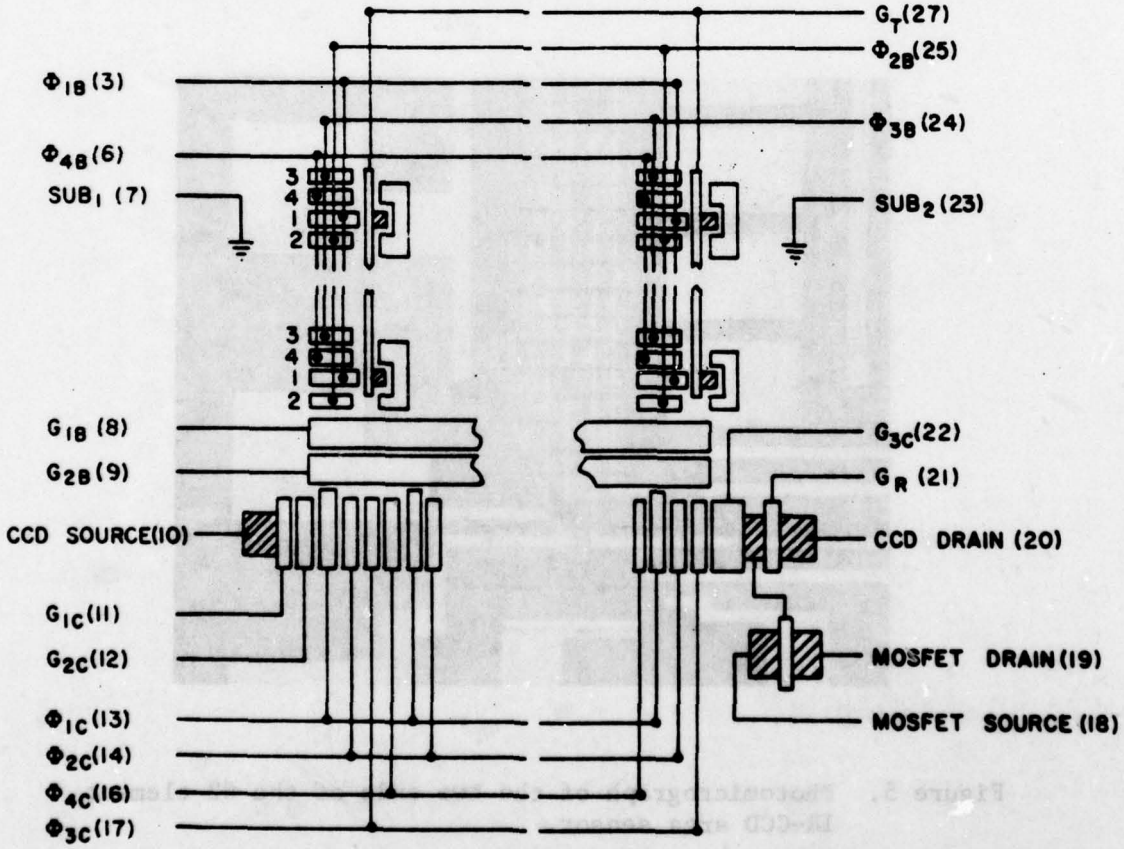


Figure 7. Schematic diagram of the 25x50-element IR-CCD area sensor (pin numbers are in parentheses).

The detailed construction of the platinum silicide Schottky-barrier detectors and the corresponding parts of the B-CCD column registers are illustrated in Fig. 8. The source-drain diffusions are shown as dashed lines, while the channel-stop diffusions are crosshatched. Hidden lines are omitted for clarity, but are shown in cutaway section. The solid polygons are labeled according to the key in the figure. Shown in this figure is the four-phase, vertical-column shift register constructed with two levels of polysilicon gates. The first-level gates are 0.9 mil long in the direction of the channel. The length of the second-level gates over the channel oxide is 0.7 mil, but their length, including overlap, is 0.9 mil. Thus, one stage of the column register, corresponding to the vertical spacing of the picture elements, is 3.2 mil. The horizontal spacing between the picture elements of this area sensor is 6.4 mil.

As is illustrated in Figs. 4, 7, and 8, the polysilicon gates of the column registers are connected to the four-phase clocks by vertical aluminum buses that, in turn, are linked at the top of the chip to the clocks ϕ_{1B}, ϕ_{2B}, ϕ_{3B}, and ϕ_{4B}. This layout of the column registers was chosen to maximize the area for the platinum silicide detectors.

The transfer of charge from the column registers to the horizontal-output register is accomplished by the gates G_{1B} and G_{2B} shown in Fig. 7. The detailed layout of this transfer structure is shown in Fig. 9, which is shown with the same scheme as Fig. 8. Although not explicitly illustrated in this figure, the separation between the adjacent vertical column registers in the area sensor is 6.4 mil. To avoid very long gates, the four-phase, horizontal-output register was designed with two 3.2-mil-long register stages between the successive vertical column registers. The first-level polysilicon gates of the horizontal-output register are 0.8 mil long. The actual length of the second-level polysilicon gates over the channel oxide is also 0.8 mil, but the total length of these gates is 1.2 mil with 0.2-mil overlap on each side of the first-level gates.

As has been shown in Fig. 7, the horizontal-output register is powered by four-phase clocks ϕ_{1C}, ϕ_{2C}, ϕ_{3C}, and ϕ_{4C}. The gates G_{1C} and G_{2C} in conjunction with the CCD source are used to introduce a bias charge (fat zero) to the output register. The output is derived from a floating diffusion that

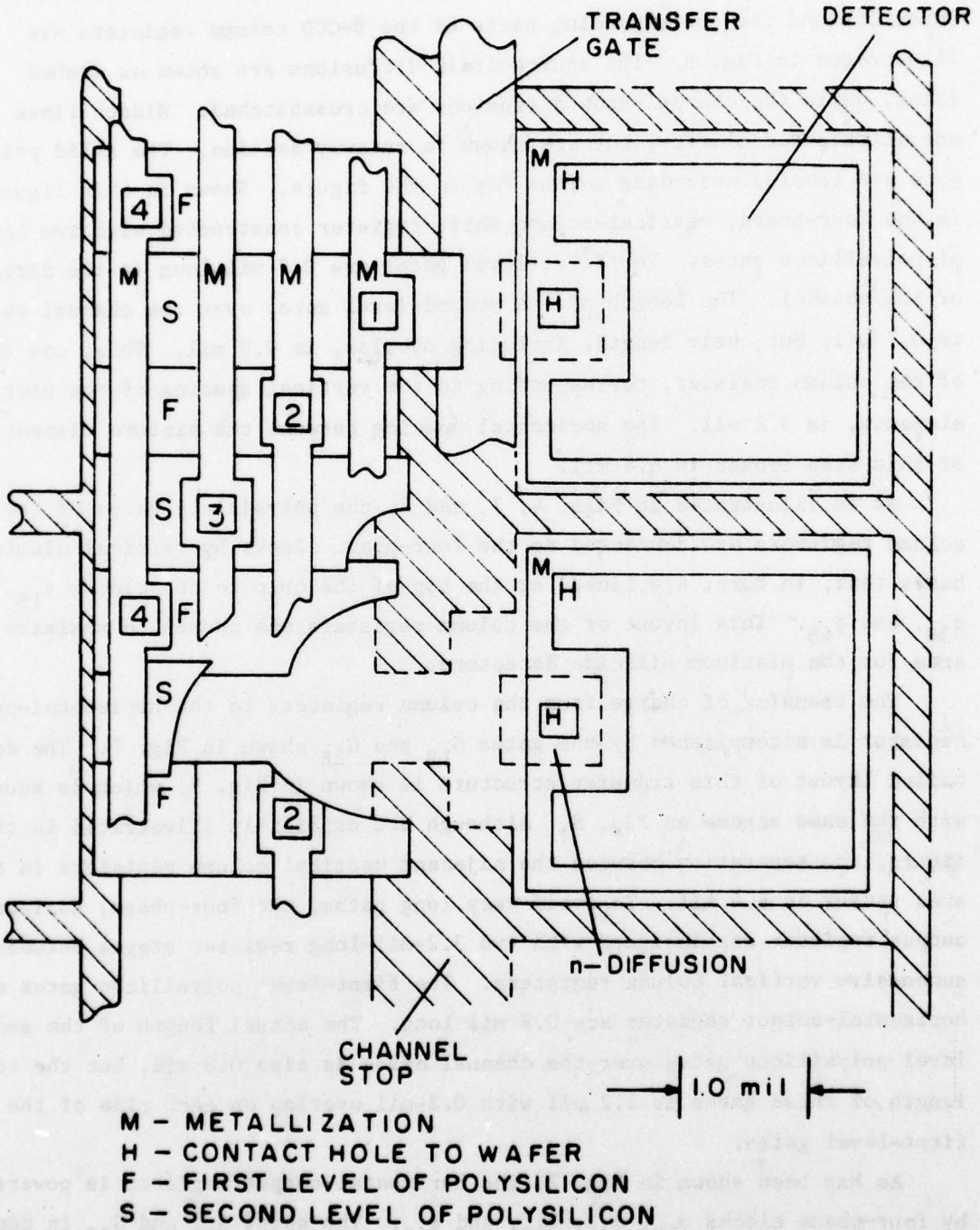


Figure 8. Scale drawing of vertical shift register adjacent to two detectors.

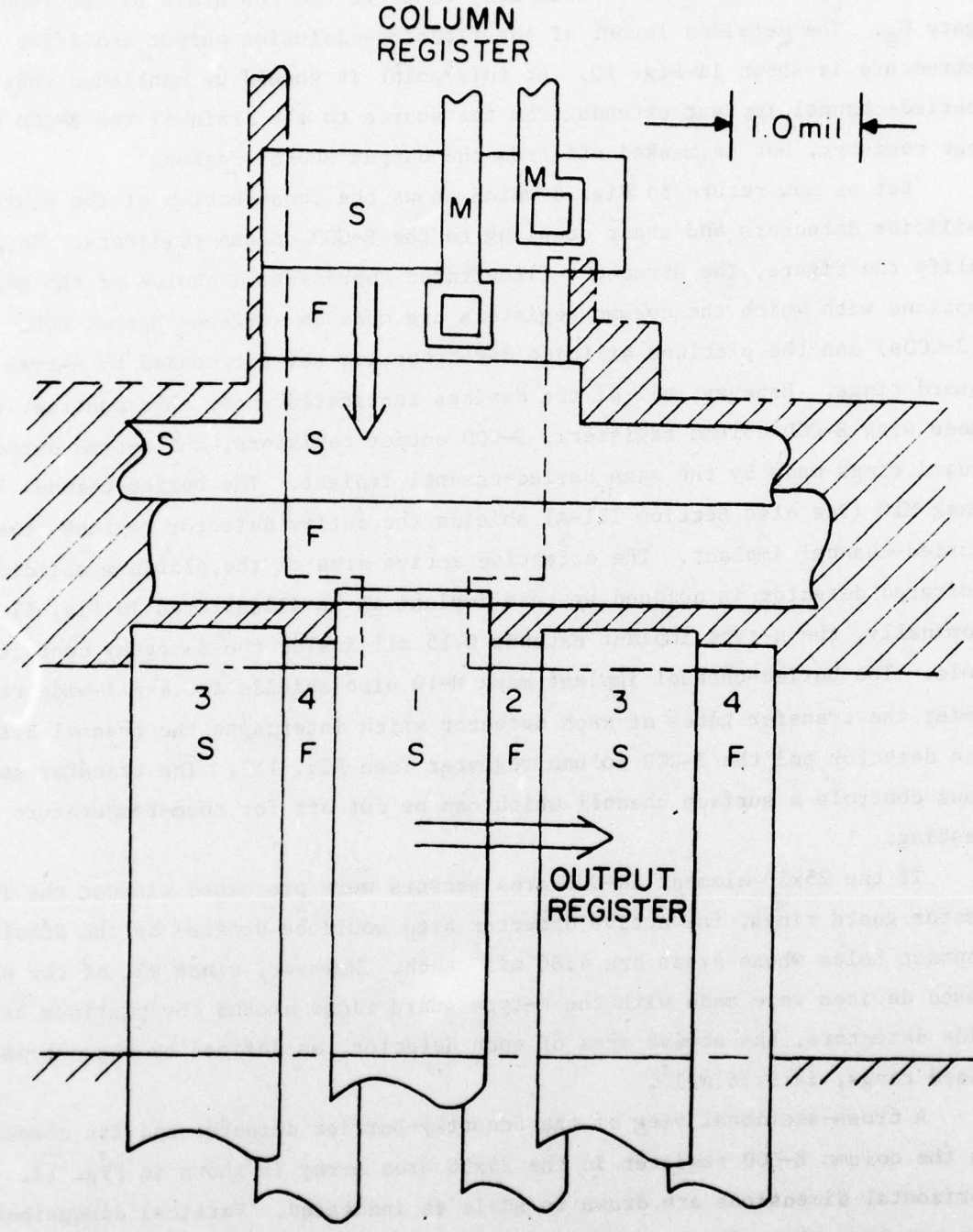


Figure 9. Scale drawing of column-register to output-register transfer structure.

is isolated from the output-register clocked gates by a dc-biased gate G_{3C}. The floating diffusion is periodically reset to the CCD drain by the reset gate G_R. The detailed layout of the floating-diffusion output amplifier structure is shown in Fig. 10. At this point it should be mentioned that the buried-channel implant extends from the source to the drain of the B-CCD output register, but is masked off from the output MOSFET region.

Let us now return to Fig. 8 which shows the construction of the platinum silicide detectors and their coupling to the B-CCD column registers. To simplify the figure, the structure illustrated represents a choice of the mask options with which the column registers are made as surface-channel CCDs (S-CCDs) and the platinum silicide detectors are not surrounded by n-type guard rings. However, all of the devices fabricated under this contract were made with B-CCD column registers, B-CCD output registers, and n-type detector guard rings made by the same buried-channel implant. The buried-channel implant mask M10 (see also Section III-A) shields the active detector regions from the buried-channel implant. The effective active area of the platinum silicide infrared detector is defined by this implant as is illustrated in Fig. 11. Nominally, the n-type implant extends 0.15 mil inside the Schottky contact hole. The buried-channel implant mask M-10 also shields a 0.4-mil-wide region under the transfer gates at each detector which intercepts the channel between the detector and the B-CCD column register (see Fig. 11). The transfer gate thus controls a surface channel which can be cut off for room-temperature testing.

If the 25x50-element IR-CCD area sensors were processed without the detector guard rings, the active detector area would be defined by the Schottky contact holes whose areas are 4.86 mil^2 each. However, since all of the processed devices were made with the n-type guard rings around the platinum silicide detectors, the active area of each detector, as defined by the n-type guard rings, is 3.36 mil^2.

A cross-sectional view of the Schottky-barrier detector and its coupling to the column B-CCD register in the 25x50 area array is shown in Fig. 12. Horizontal dimensions are drawn to scale as indicated. Vertical dimensions are not to scale. The buried-channel implant is shown under the shift-register gates, and surrounding the detector as a guard ring. There is no implant under

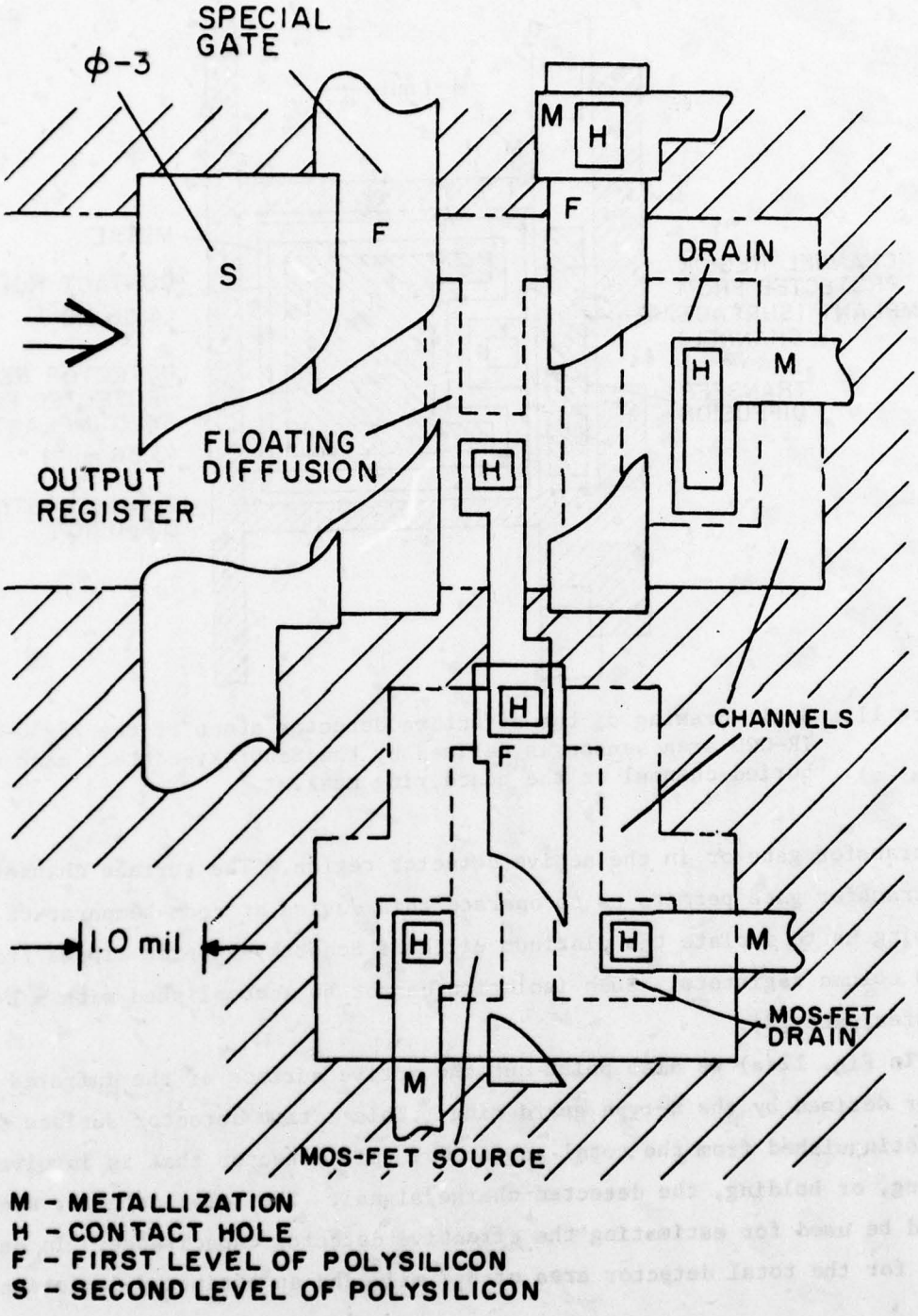


Figure 10. Scale drawing of the floating-diffusion output amplifier.

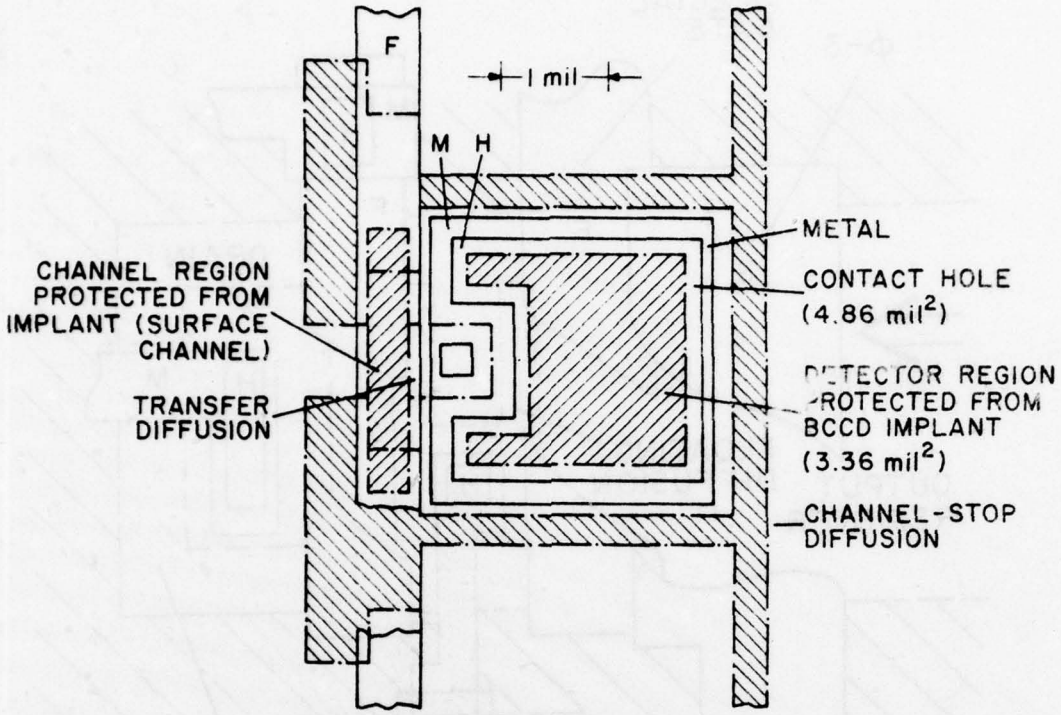


Figure 11. Scale drawing of the effective detector areas of the 25x50-element IR-CCD area sensor as defined by the Schottky-contact mask and the buried-channel or the guard ring mask.

the transfer gate or in the active detector region. The surface channel under the transfer gate permits us to operate this device at room temperature by allowing us to isolate the platinum silicide Schottky-barrier diodes from the B-CCD column registers. Such isolation cannot be accomplished with a B-CCD transfer gate [2].

In Fig. 12(a) we also point out the active surface of the infrared detector defined by the n-type guard ring. This active detector surface should be distinguished from the total surface of this detector that is involved in storing, or holding, the detected charge signal. The total detector area should be used for estimating the effective detector capacitance. In our case, for the total detector area of 8.7 mil^2 and an estimated depletion-layer

2. W. F. Kosonocky and J. E. Carnes, "Basic Concepts of Charge-Coupled Devices," RCA Review 36, 566-593, Sept. 1975.

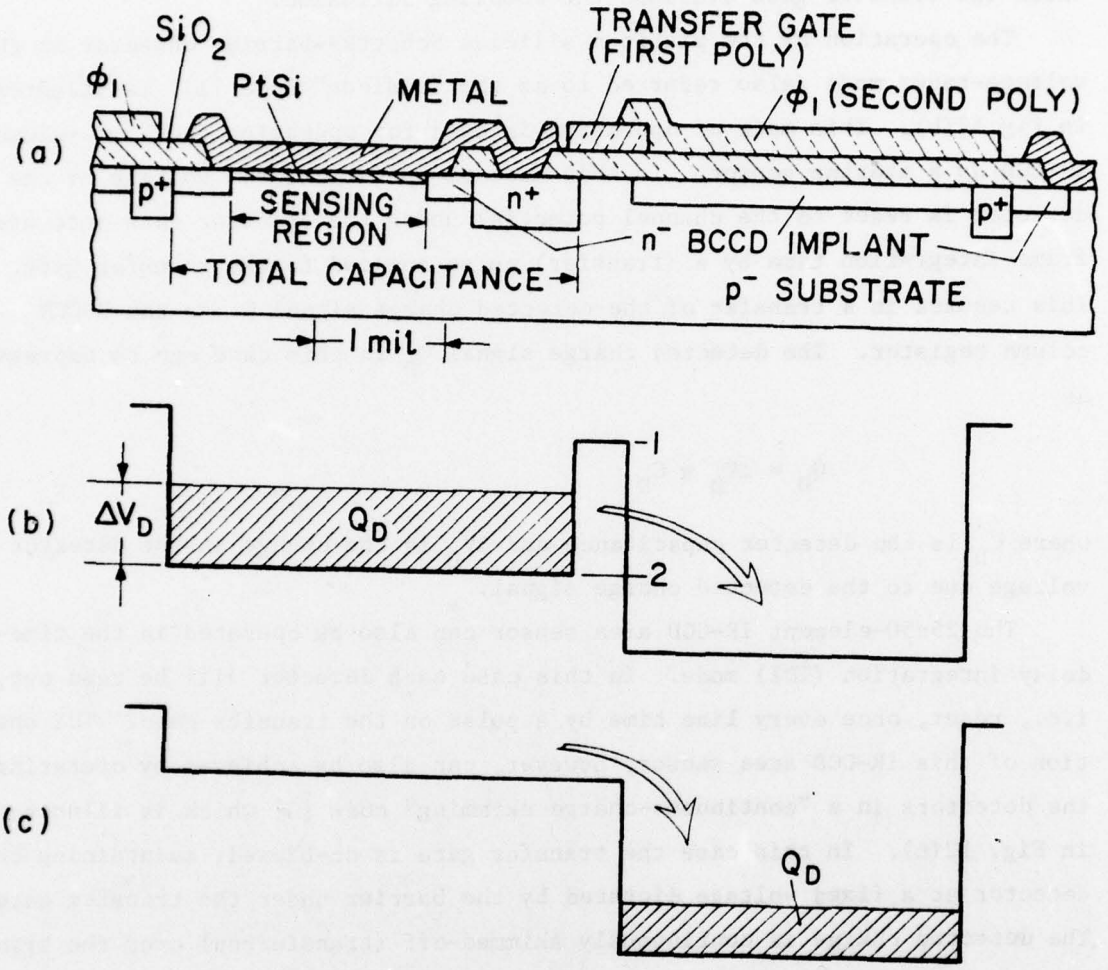


Figure 12. Construction and operation of area-array detectors: (a) cross section of area sensor showing detector region, transfer structure and shift-register gate. (b) electron-energy profile during voltage-reset operation of detector; (c) electron-energy profile during continuous-skimming operation.

capacitance per unit area of 0.04 pF/mil^2, the detector capacitance can be estimated to be 0.4 pF. This number includes 0.056 pF of oxide capacitance where the transfer gate overlaps the coupling diffusion.

The operation of the platinum silicide Schottky-barrier detector in the voltage-reset mode (also referred to as the "vidicon" mode [1]) is illustrated in Fig 12(b). This mode of operation is used for operating the 25x50-element IR-CCD as a staring sensor. In this mode of operation, the voltage of the detector is reset to the channel potential under the transfer gate once every frame-integration time by a (transfer) pulse applied to the transfer gate. This results in a transfer of the detected charge signal Q_D to the B-CCD column register. The detected charge signal Q_D in this case can be expressed as

$$Q_D = \Delta V_D \times C_D \tag{1}$$

where C_D is the detector capacitance and ΔV_D is the change in the detector voltage due to the detected charge signal.

The 25x50-element IR-CCD area sensor can also be operated in the time-delay integration (TDI) mode. In this case each detector will be read out, i.e., reset, once every line time by a pulse on the transfer gate. TDI operation of this IR-CCD area sensor, however, can also be achieved by operating the detectors in a "continuous-charge skimming" mode [3] which is illustrated in Fig. 12(c). In this case the transfer gate is dc-biased, maintaining the detector at a fixed voltage dictated by the barrier under the transfer gate. The detected charge is continuously skimmed-off (transferred) over the transfer barrier into the column register.

C. DESIGN AND OPERATION OF THE 62-ELEMENT IR-CCD LINE SENSOR

The general layout of the 62-element IR-CCD line sensor was shown on the photomicrographs in Fig. 5. A schematic sketch of this line sensor including

3. W. F. Kosonocky, D. J. Sauer, and F. V. Shallcross, *256-Element Schottky-Barrier IR-CCD Line Sensor*, Final Report No. RADC-TR-77-304 under Contract No. F19628-76-C-0254, Sept. 1977.

all required electrical terminals and pin connections to a dual-in-line package is shown in Fig. 13. A scale drawing of one stage of the line sensor is shown in Fig. 14. The active area of the infrared platinum silicide detector, illustrated in Fig. 15, is similar to the active area of the detectors of the area sensor. The active detector area for the line sensor constructed without the n-type guard ring is 7.2 mil^2. However, for the case where the n-type guard rings are formed around the detectors, the effective detector area is 5.0 mil^2.

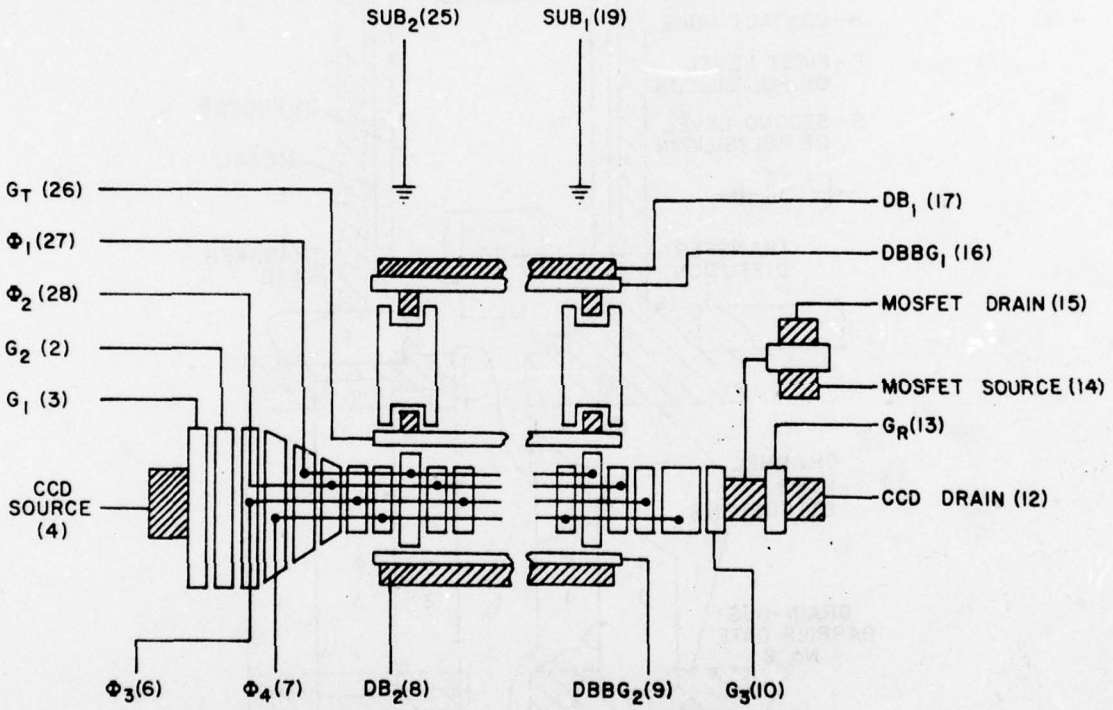


Figure 13. Schematic diagram of the 62-element IR-CCD line sensor (pin numbers are in parentheses).

The construction of the 62-element IR-CCD line sensor is very similar to the construction of one column of the 25x50-element IR-CCD area sensor. For both cases the detectors are placed on 3.2-mil centers. The line sensor, however, was designed not only to simulate one column of the area sensor, but also to test two types of background-subtraction schemes. Therefore, the detector areas of the line sensor turned out to be somewhat different from the detector areas of the area sensor. As can be observed in Figs. 5, 13, and 14,

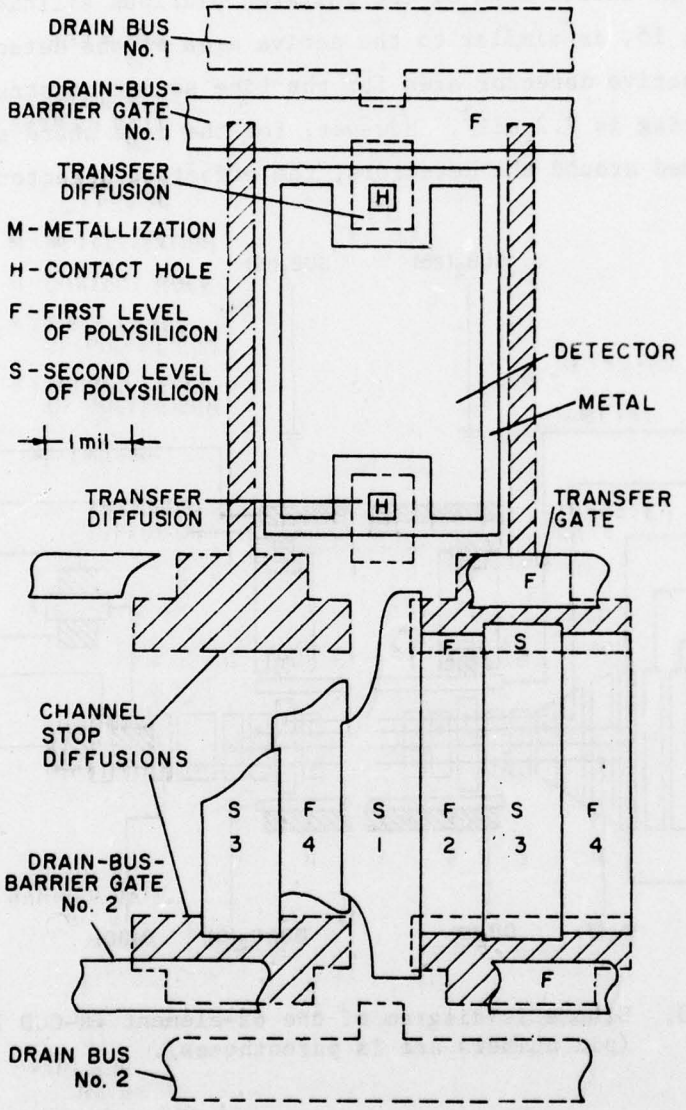


Figure 14. Scale drawing of one stage of the 62-element IR-CCD line sensor.

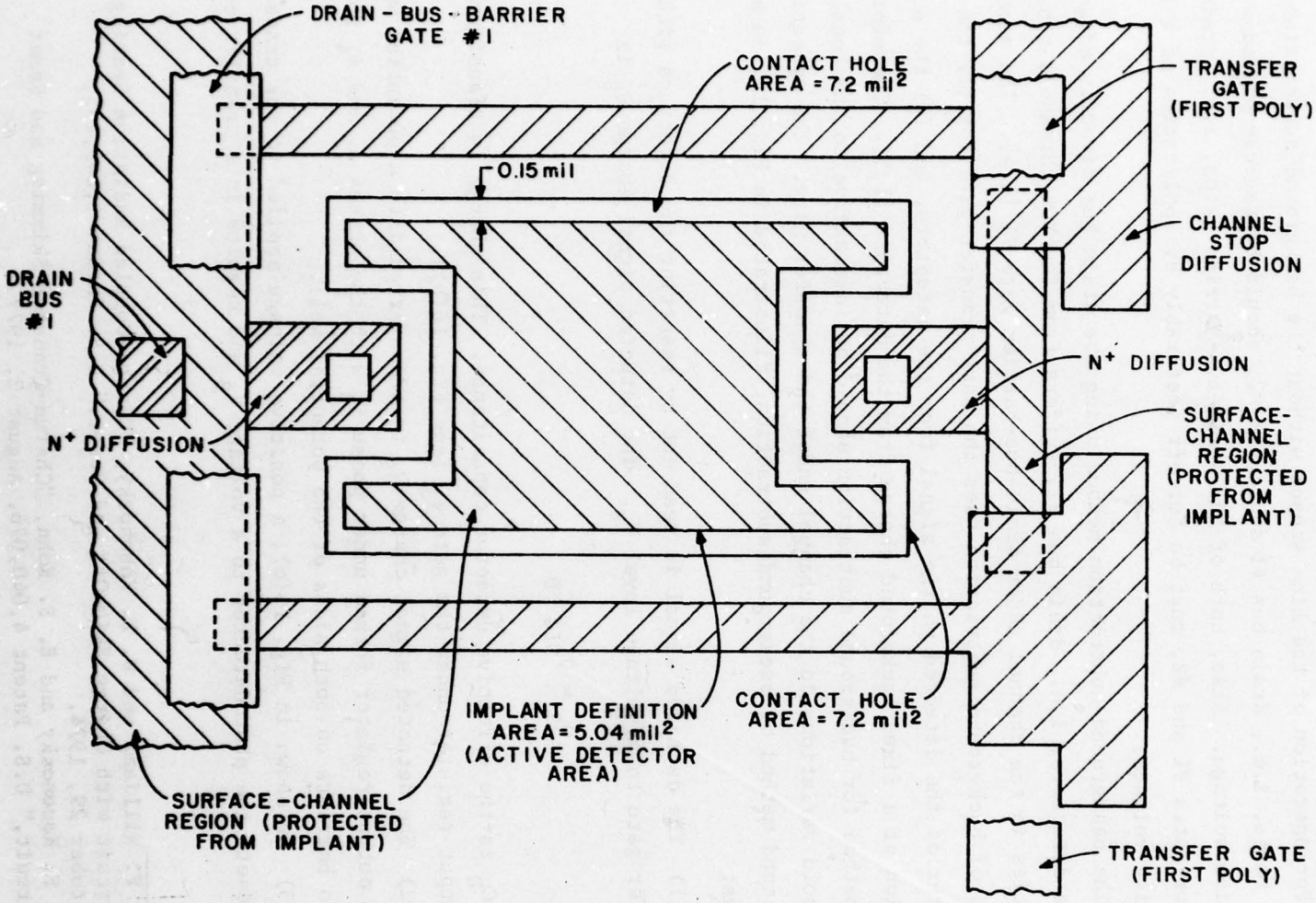


Figure 15. Detailed scale drawing of a detector in the 62-element IR-CCD line sensor, showing its coupling to the shift register and to the drain bus #1, and the region shielded from the B-CCD implant.

the line sensor is surrounded on both sides by two types of drain structures to test the two methods for background subtraction.

For operation of the line sensor without the background subtraction, both drain buses, i.e., drain bus #1 and drain #2, should be reverse-biased with a positive voltage. Also, both of the drain-bus-barrier gates, i.e., drain-bus-barrier gates #1 and #2, must be cut off preferably by application of a large negative voltage.

The background-subtraction method using the drain bus directly adjacent to the detectors, i.e., drain bus #1, suffers from the MOS-threshold nonuniformities in the channel under drain-bus-barrier gate #1 [1,4]. The second method of background subtraction uses the same transfer gate for (1) the transfer of the detected charge signal from the detectors, and (2) the subtraction of a fixed background charge from the detectors [1,5]. Therefore, this method for background subtraction should be insensitive to the local MOS-threshold variations in the channel under the transfer gate. The operation of the second method of background subtraction, illustrated in Fig. 16, is as follows:

(1) The detected signal is read out by resetting the detectors with the transfer gate to a voltage level V_S. The detected signal charge Q_S is

$$Q_S = V_{SIG} C_D \tag{2}$$

where C_D is the effective detector capacitance. This charge is transferred to the output register under the gate ϕ_1 (see Fig. 16(b)).

(2) The detected signal charge Q_S is transferred into a potential well in the output register formed under phase ϕ_3 with the phases ϕ_2 and ϕ_4 forming the two barriers on both sides of the potential well.

(3) As shown in Fig. 16(c), a positive voltage applied to the transfer gate resets the photodetector to a voltage V_B and results in a transfer of the

4. B. F. Williams and W. F. Kosonocky, "Charge-Coupled Radiation Sensing Circuit with Charge Skim-Off and Reset," U.S. Patent 3,845,295, October 29, 1974.
5. W. F. Kosonocky and E. S. Kohn, "Charge-Transfer Skimming and Reset Circuit," U.S. Patent 4,040,076, August 2, 1977.

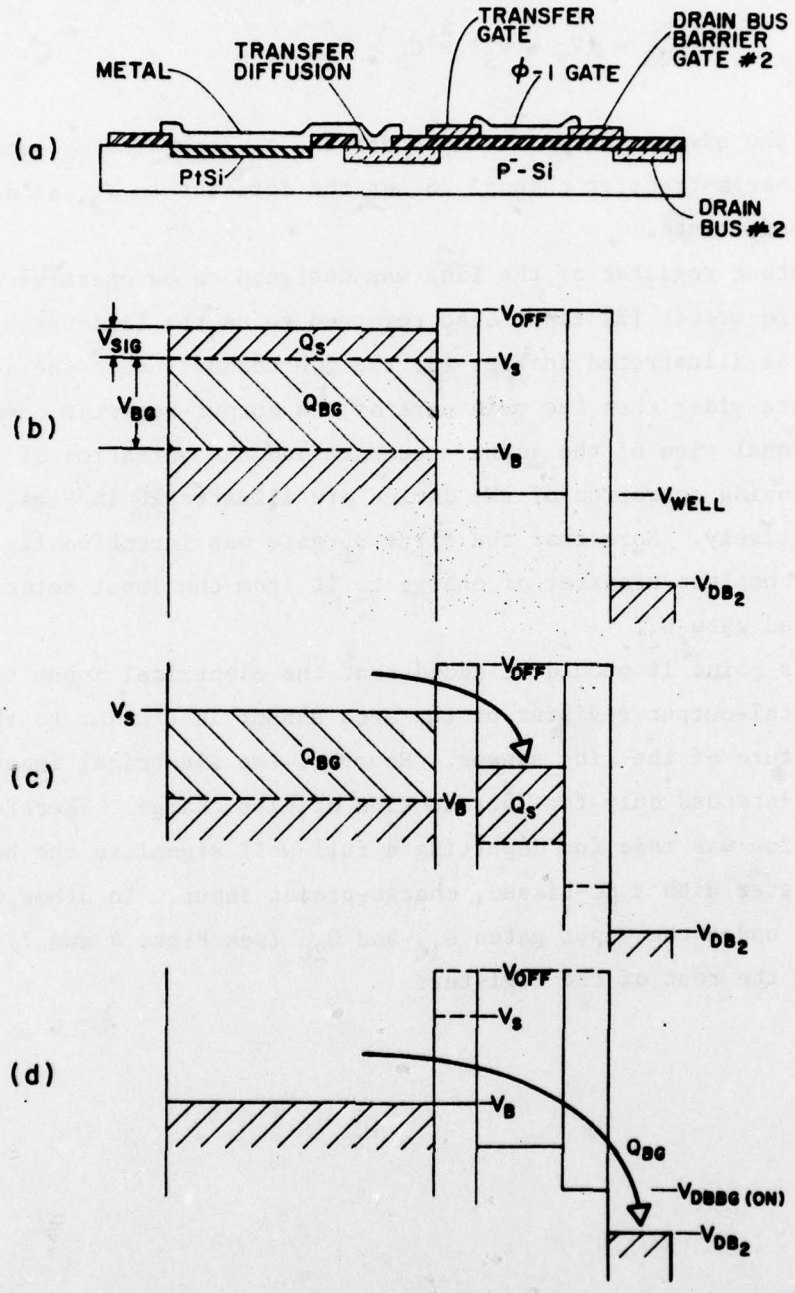


Figure 16. Construction and operation of the background-subtraction structure that is insensitive to the MOS-threshold variations under the transfer gate. (a) Cross-sectional view of structure; (b) Profile at the end of storing time, but before transfer; (c) Transfer of signal charge to shift register; (d) Transfer of background charge to drain bus #2.

background charge to the drain bus #2. The drain-bus-barrier gate #2 is biased on during this time. The background charge Q_{BG} removed may be expressed as

$$Q_{BG} = (V_B - V_S) \times C_D = V_{BG} \times C_D \qquad (3)$$

Thus, with the signal charge stored under the ϕ_3 gate, the ϕ_1 gate is being used as a charge-transfer channel to set the detector to V_B, as determined by the transfer gate.

The output register of the line was designed to be operated with a dc-biased charge-preset [2] input also referred to as the fill-and-spill input. Therefore, as illustrated in Fig. 13, the CCD channel under the input gates G_1 and G_2 are wider than the main part of the output-register channel. The cross-sectional view of the input structure and the variation of the channel potential during operation of the device are illustrated in Figs. 17(a) and (b), respectively. Note that the first ϕ_1 gate was intentionally made longer to allow a complete transfer of charge to it from the input metering well under the dc-biased gate G_2.

At this point it should be added that the electrical input structure of the horizontal-output register of the area sensor is similar to the electrical input structure of the line sensor. However, the electrical input of the area sensor was intended only for introduction of bias charge. Therefore, no special provision was made for inputting a full-well signal to the horizontal-output register with a dc-biased, charge-preset input. In other words, the CCD channel under the input gates G_{1C} and G_{2C} (see Figs. 4 and 7) is the same width as in the rest of the register.

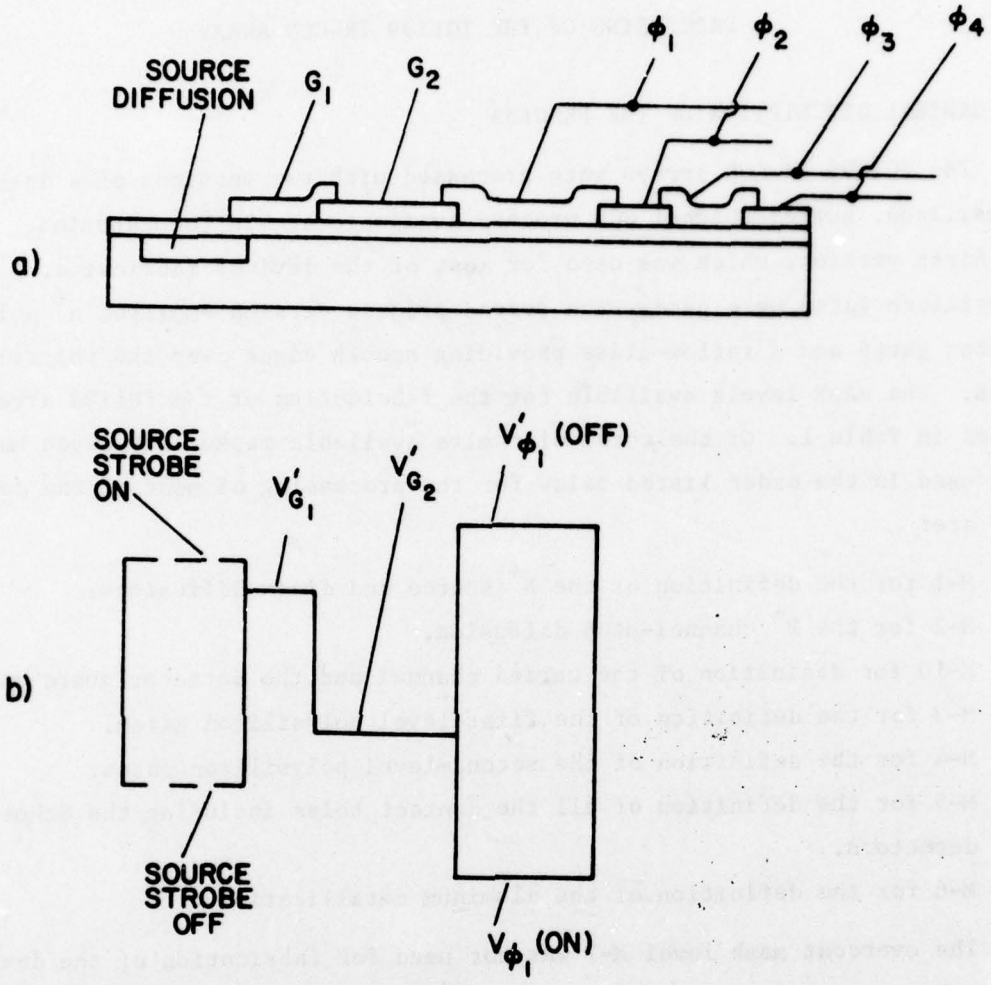


Figure 17. Construction and operation of the input circuit for the 62-element IR-CCD line sensor. (a) Cross-sectional view. (b) Corresponding potential-energy profile.

SECTION III

PROCESSING OF THE TC1199 IR-CCD ARRAY

A. GENERAL DESCRIPTION OF THE PROCESS

The TC1199 IR-CCD arrays were processed with two versions of a double-polysilicon, buried-channel CCD process available at RCA Laboratories. In the first version, which was used for most of the devices fabricated, p^+ polysilicon gates were used. The second-process version employed n^+ polysilicon gates and a reflow-glass providing smooth edges over the polysilicon gates. The mask levels available for the fabrication of the TC1199 array are listed in Table 1. Of the total of twelve available masks only seven masks were used in the order listed below for the processing of most of the devices. They are:

(1) M-1 for the definition of the N^+ source and drain diffusions.
(2) M-2 for the P^+ channel-stop diffusion.
(3) M-10 for definition of the buried channel and the detector guard rings.
(4) M-3 for the definition of the first-level polysilicon gates.
(5) M-4 for the definition of the second-level polysilicon gates.
(6) M-5 for the definition of all the contact holes including the Schottky detectors.
(7) M-6 for the definition of the aluminum metallization.

The overcoat mask level M-7 was not used for fabrication of the devices under this contract because we found in the previous work that by careful handling of the processed chips we did not suffer any appreciable yield loss in finished devices. The deposition of SiO_2 as the scratch-protection overcoat introduced additional heat treatment following the deposition of aluminum over the platinum silicide detectors. In processing the IR-CCD arrays we wanted to avoid this additional heat treatment.

The contact-hole mask M-8, which does not include the contacts for the Schottky detectors, in conjunction with a separate mask level M-9, for the definition of the detector contact holes were prepared to provide additional flexibility for the development and optimization of the device process. The definition of the contact holes by the combination of the mask levels M-8 and M-9 was done for the processing of the TC1199 arrays with N^+ polysilicon gates.

TABLE 1. TC1199 MASK LEVELS

(1) M-1. Source-drain diffusion.

(2) M-2. Channel-stop diffusion.

(3) M-3. First-poly definition.

(4) M-4. Second-poly definition.

(5) M-5. All contact holes, including detectors.

(6) M-6. Metal definition.

(7) M-7. Holes in SiO_2 overcoat for bonding.

(8) M-8. Contact holes, except detectors.

(9) M-9. Detector holes.

(10) M-10. Implant definition for buried channels and guard rings.

(11) M-11. Implant definition for buried channels only.

(12) M-12. Implant definition for guard rings only.

All of the devices made under this contract were made with a single phosphorus implant to form the buried-channel CCD regions and the n-type guard rings for the platinum silicide detectors. For this we have used the single mask level M-10. To allow for additional processing flexibility, we prepared the separate mask levels M-11 for the definition of the buried-channel implant, and M-12 for an independent implant for the formation of the n-type guard rings surrounding the platinum silicide detectors. Of course, for the surface-channel version of the TC1199 arrays, neither of the buried-channel masks M-10 or M-11 would be used. However, we could still implant the n-type guard rings using the mask level M-12.

The TC1199 devices were processed using 25-50 Ω-cm, boron-doped, p-type [100] silicon wafers polished on both sides to a final thickness of 0.010 in. by Monsanto.* Some wafers, however, were also repolished on the back sides

*Monsanto Co., St. Peters, MO.

at RCA Laboratories. This was normally done after the deposition, but before the definition of the aluminum. A 500-Å-thick film of platinum was deposited on the wafer with the Schottky contact holes opened in a magnetron-sputtering system. One of the three following procedures was used to form the platinum silicide:

(1) Sintering at 650°C for 10 min followed by a 20-min hydrogen anneal.
(2) Sintering at 650°C for 30 min followed by a 20-min hydrogen anneal.
(3) Sintering and annealing at 320°C for 8 h in nitrogen, and then for another 8 h in forming gas, giving a total time at 320°C of 16 h.

After the platinum silicide formation, the remaining metallic platinum is etched, and a 14000-Å film of aluminum is deposited. In the early processing runs we also used a film of titanium as a barrier between the platinum silicide and the aluminum. However, later, we found that this additional processing step was not necessary for achieving good aluminum contacts. After the definition of the aluminum, the wafers were probe-tested, and diced. The good chips were bonded in 28-pin ceramic dual-in-line packages which were prepared with the windows shown in Figs. 2(b) and 3(b) for back-side illumination with infrared images.

B. PROCESSING VARIATIONS

Five processing lots of TC1199 IR-CCD arrays were fabricated during the contact period. The process variations selected for the formation of the platinum silicide detectors for these five wafer lots are summarized in Table 2.

The "first" and "second" wafer lots were processed with P^+ polysilicon gates. The main difference between these two lots is that we used the titanium aluminum metallization for the "first" lot. However, the "second" lot as well as all the other lots were processed with only aluminum metallization.

The "third" lot is the only lot processed with N^+ polysilicon gates. For this lot we used our reflow glass process which required the use of masks M-8 and M-9 for the contact definition. The wafers B, C, D, and G of this lot were also repolished on the back surface after the aluminum deposition step.

TABLE 2. PROCESS VARIATIONS

First Lot	1199-3	Sintered 650°C/10 min + 530°C/20 min
Second Lot	1199-4	Sintered 650°C/10 min + 530°C/20 min
Third Lot	1199-5	
	Wafers A,B,D,& F	Sintered 320°C/16 h
	Wafers C,E,& G	Sintered 650°C/10 min + 530°C/20 min
Fourth Lot	1199-6	
	Wafers A,B,C,& D	Sintered 650°C/30 min + 530°C/20 min
	Wafers E,F,& G	Sintered 320°C/16 h
Fifth Lot	1199-7	
	Wafers A,B,C,D	Sintered 650°C/30 min + 530°C/20 min
	Wafers E,F,G,& H	Sintered 320°C/16 h

Both the "fourth" and the "fifth" wafer lots were fabricated with P^+ polysilicon gates. In the "fourth" wafer lot we experimented with the use of Si_3N_4 film for the protection of the back surface during the process. Our experiment, however, concluded that the deposited SiO_2 gives us better results. In the "fifth" wafer lot we back-polished all the wafers after the aluminum deposition step. The high-temperature sintering of the platinum silicide was increased in the "fourth" and the "fifth" lot to 30 min to assure a complete conversion of the platinum into the platinum silicide. This was done at the suggestion of RADC/ESE.

SECTION IV

ELECTRICAL AND OPTICAL MEASUREMENTS

A. PROBE TESTING OF IR-CCD WAFERS

Both dc and ac methods were found useful for probe-testing of the IR-CCD wafers. The ac method, which consisted of operating all of the CCD registers at room temperature with the platinum silicide diodes isolated by the (interline) transfer gate, was found most useful when the processing yield was good. However, in the case of wafers with very low yield, the dc probe-testing approach was more effective for diagnosing the yield problems. In our best wafer runs, the yield of the 25x50-element IR-CCD area sensor was about 20 percent, i.e., corresponding to 8 to 10 operable area arrays for a possibility of 45 chips per wafer. The yield for the line arrays was better than for the area arrays, but it is not specified here because the chips with good area devices were not tested for line-array performance.

The ac probe-testing of the area arrays involved the following procedure. The (interline) transfer gate was biased off to isolate the platinum silicide detectors from the column registers. The horizontal-output register was then operated to measure the transfer efficiency with electrical input. If the transfer efficiency was good, then the B-clock amplitude was turned up to operate the column registers while the wafer was partially uncovered to permit small response of the output signal to room light. The integration time was then increased from 1/60 s to 1/30 and 1/15 s. If the video signal doubled at each step, the area shift register was deemed to be working properly. The wafer was then covered again, and the transfer-gate bias was varied to determine the voltage level at which the column registers started being loaded with dark current from the platinum silicide detectors. Area arrays that pass all these tests were identified as acceptable for mounting. Some area arrays had large dark current when the B-clock was turned up. These were accepted, only if they permitted operation of the B-clock to at least 8 V without excessive dark current. This dark current may be substantially reduced when the samples are cooled. Line-array, ac testing involved testing of transfer efficiency and transfer gate action only.

When reasonable yields were obtained, ac probe-testing was faster and more critical of performance. However, when yield was very low, ac probe-testing did not identify the problem. DC probing usually showed the problem to be short-circuited gates. Several times we redefined the metal and re-etched, resulting in an improved yield. The ac test was then repeated to identify chips suitable for mounting.

B. B-CCD REGISTER TRANSFER LOSS AT 77 K

As in our previous work with the 256-element IR-CCD line sensor [3] the B-CCD transfer loss measurements indicated larger charge-trapping transfer losses at 77 K than are normally measured at room temperature. Typical transfer-loss measurements illustrated in Figs. 16(a) and (b) show the comparison between room-temperature operation and operation at 77 K, respectively. At room temperature, with no intentional bias charge applied, the transfer losses are too small to be measured, i.e., approximately in the range of 10^{-5} per transfer. At 77 K, without bias charge, the transfer loss was about 4×10^{-4} per transfer (see the output waveform on the left in Fig. 18(b)). However, with introduction of a bias charge (see the output waveform on the right in Fig. 18(b)) the transfer loss decreased to 8×10^{-5} per transfer. To obtain the above numbers for the measured transfer losses we divided the observed loss by 250 transfers, which are involved in operating the output register of the 62-element line sensor with a four-phase clock.

C. SIGNAL-HANDLING CAPACITY OF THE INFRARED DETECTORS

Infrared response was demonstrated with the 62-element IR-CCD line sensors. The sample line-array package was operated at the end of a dipstick under liquid nitrogen in a quartz dewar. The sample and dipstick were protected by a plastic bag. Infrared light from a germanium-filtered tungsten lamp illuminated the chip from the back side. Because of the poor optics and the incomplete IR transmission of the elements in the optical path, imaging was not attempted, nor were quantitative measurements of detector sensitivity. The purpose of this experiment was to demonstrate IR sensitivity of the detectors, and the proper operation of the transfer gate, and to measure the signal-handling capability of the line-array detectors.

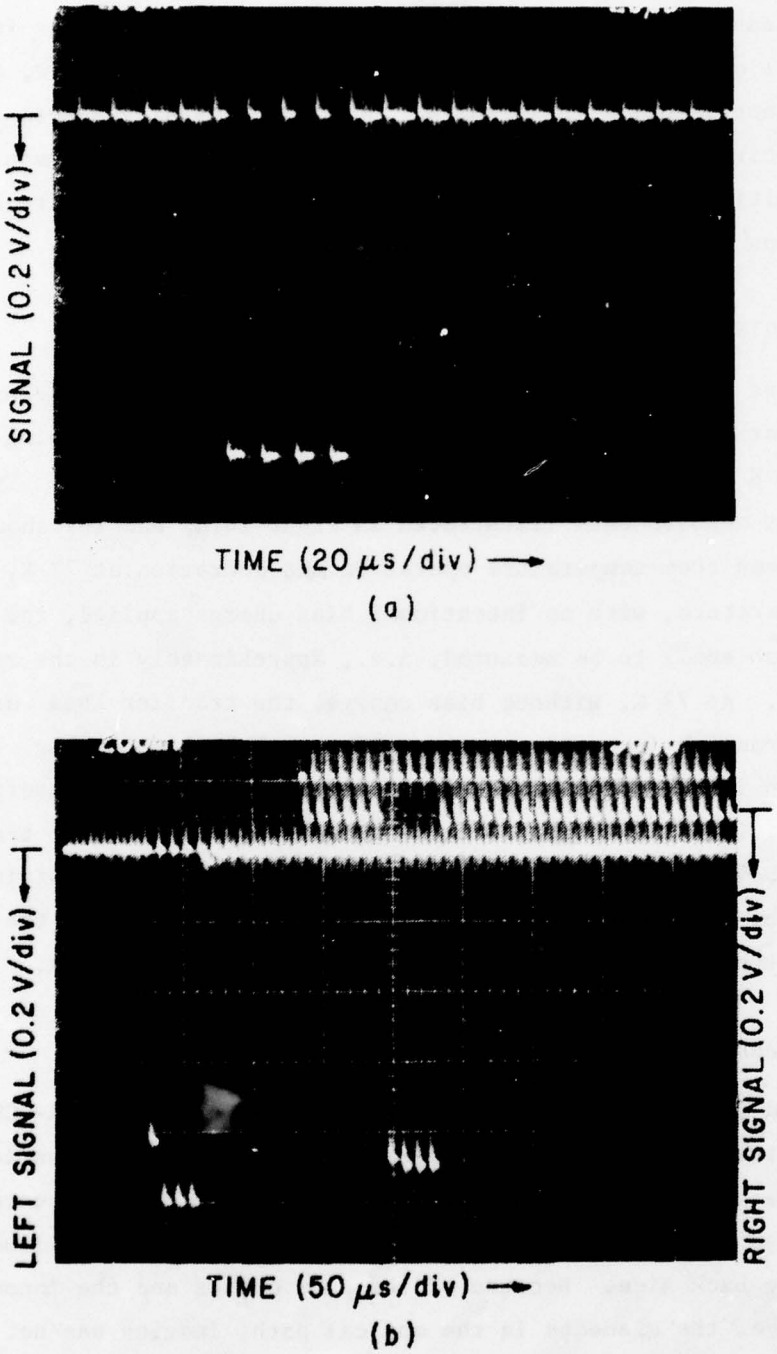


Figure 18. Shift register performance of a 62-element IR-CCD line sensor: (a) at room temperature without bias charge; and (b) at 77 K without bias charge (left side) and with a bias charge (right side).

The measurement of the signal-handling capability of the line sensor is illustrated in Fig. 19 for transfer-pulse amplitudes of 5 V, 5.5 V, and 6 V referred to a -2 V bias level. For this test the line sensor was flooded by a tungsten light filtered through germanium. At each transfer-pulse amplitude, the illumination was increased beyond the amount for which more light made no change in the pattern. The integration time was 28 ms. The signal threshold was at a pulse amplitude of 4.5 V at the right of the display and 4.8 V on the left (2.5 V and 2.8 V to substrate). This difference in transfer threshold is seen to persist as the transfer pulse is increased. The signal-handling capability is plotted as a function of pulse amplitude in Fig. 20. This signal is obtained at the output of the on-chip source follower. One volt at this point corresponds to 7×10^{-13} C in the charge packet. This is equivalent to a floating-diffusion-capacitance/source-follower-gain ratio of 0.7 pF. This number was determined by direct measurement of the drain current at 77 K with an electrical input, and observation of the output signal voltage. With a source-follower gain of 0.7, a floating-diffusion capacitance of 0.5 pF is implied.

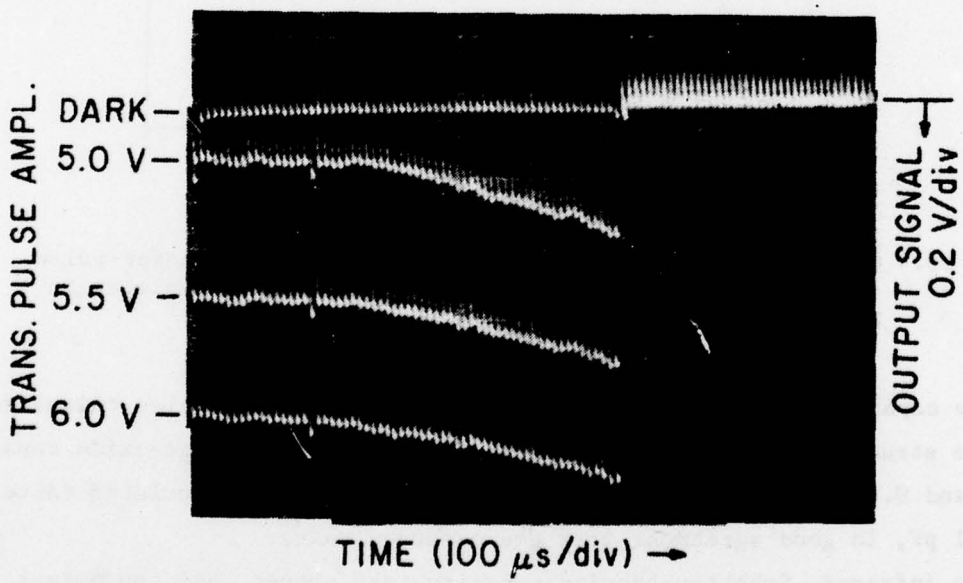


Figure 19. Output waveforms of a 62-element CCD line sensor flooded with infrared light (filtered through germanium) for several transfer-gate-pulse amplitudes on a 2-V dc bias level.

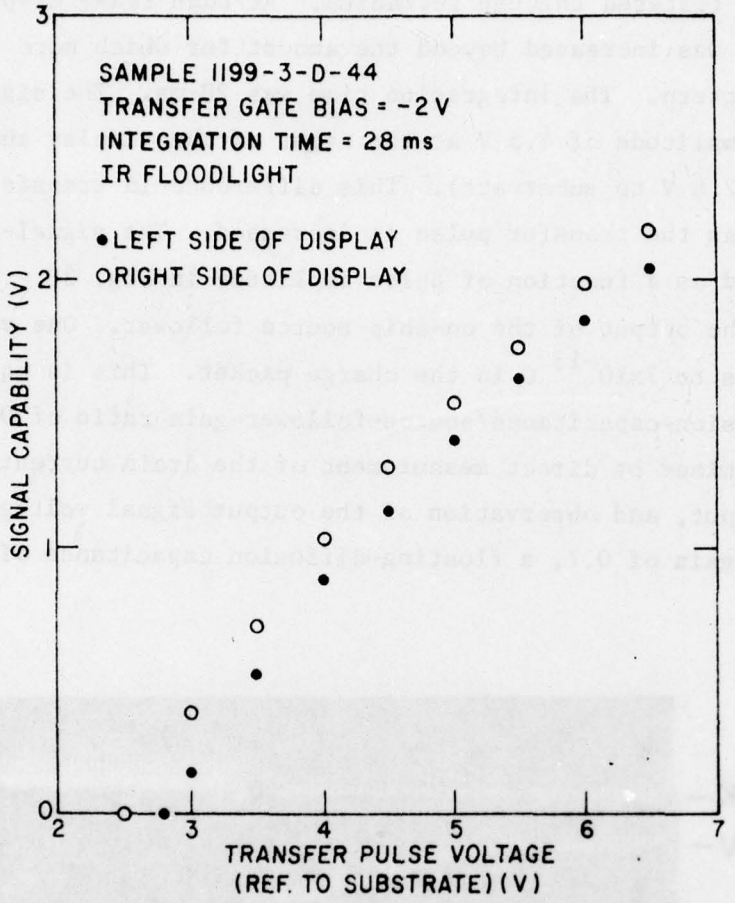


Figure 20. Graph of signal capability as a function of transfer-pulse voltage (referred to substrate) for the same sample as in Fig. 19.

The capacitance of the floating-diffusion assembly was also calculated from the structure area using the values 0.14 pF/mil^2 for gate-oxide capacitance and 0.04 pF/mil^2 for diffusion capacitance. This calculated value was 0.41 pF, in good agreement with the measured value.

The infrared, Schottky-barrier capacity test showed that the output signal was 0.765 V for a pulse, 1 V above threshold applied to the transfer gate (see Fig. 20). For the surface-channel transfer gate, the change in surface potential is 0.9 times that applied to the gate, and the detectors are

set to that surface potential. Thus, the output changed by 0.765 V for a 0.9-V change at the detector. The detector capacitance is thus given by

$$C_D = \frac{0.765}{0.9} C_{OUT} = 0.85 \times 0.7 \text{ pF} \approx 0.6 \text{ pF}$$

The same detector capacitance calculated from the design plans was 0.55 pF using 0.14 pF/mil^2 for the oxide capacitance, and 0.04 pF/mil^2 for the depletion-layer capacitance. This agreement is quite good.

Referring back to Fig. 19 we see a rather large variation of the detected output signal (from left to right) that is interpreted as a variation of the MOS-threshold voltage along the transfer gate. Similar waveforms obtained with another line sensor are shown in Fig. 21. As is seen in this figure, the saturated-signal output waveform in this case is somewhat more uniform than in Fig. 20. At this point we would like to stress that, as demonstrated in our earlier work [1], good IR uniformity may be obtained even if the saturated signal, representing the signal-handling capabilities of the detectors, is nonuniform. The large variation of the response at transfer-gate pulse

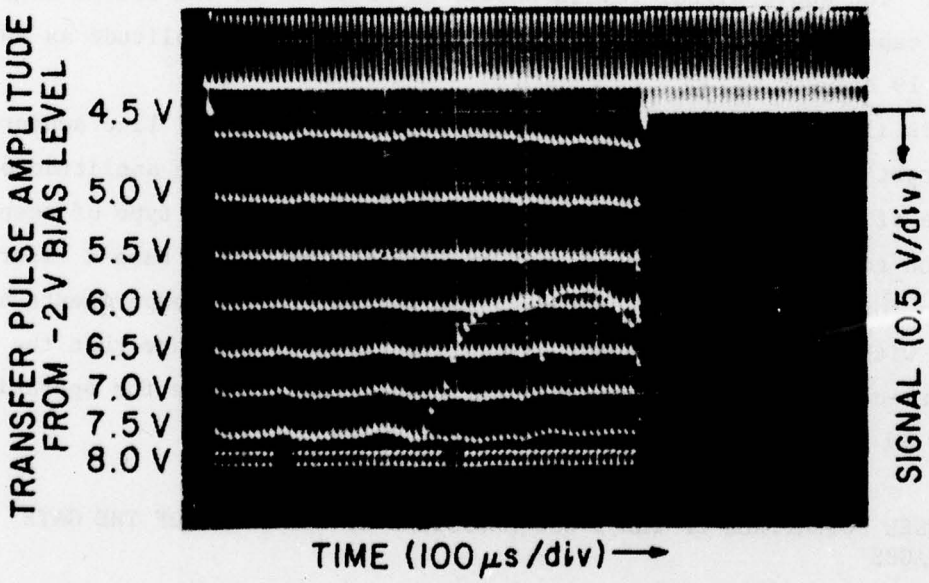


Figure 21. Signal capacity for an IR-flooded sensor at several transfer-pulse amplitudes referred to a -2 V bias level at 77 K for integration time of 28 ms.

amplitude of 7.5 V was caused by a nitrogen gas bubble. Uniformity measurements made with good infrared optics at RADC/ESE achieved uniformity in operation of the 25x50-element IR-CCD area sensor of about 1.0 percent rms.*

D. PLATINUM SILICIDE DETECTOR DARK CURRENT AT 77 K

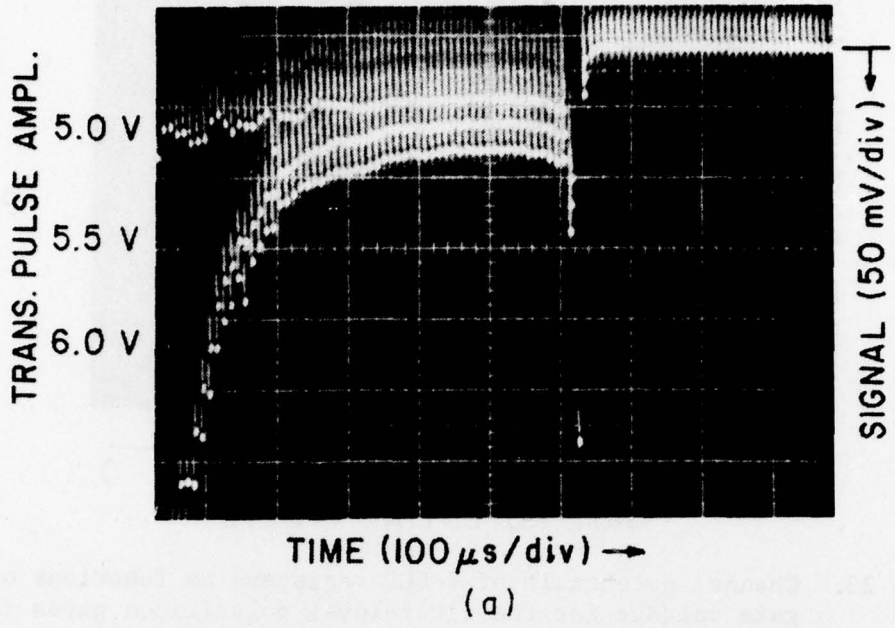
Typical waveforms of the dark-current output obtained for the 62-element IR-CCD line sensors operated at 77 K are shown in Figs. 22(a) and (b). The dark-current output waveform in Fig. 22(a) is for the same sample as the detector signal-handling capacity data shown in Figs. 19 and 20, while the waveform in Fig. 22(b) is for the same device as the data in Fig. 21. The samples were cold-shielded for these measurements by being wrapped in aluminum foil before immersion in liquid nitrogen. The dark signal varied linearly with integration time, as expected. The dark-current output was measured for various transfer-gate pulses amplitudes with a -2 V dc bias level. Note in Fig. 22(a), that for the transfer pulse of 5 V we see a dark-current output signal of 40 mV for an integration time of 0.52 s, corresponding to 2.3 mV at 30 ms. The above signal levels should be compared to the 150-mV signal-handling capability of this array at this transfer-pulse amplitude as shown in Figs. 19 and 20.

As is illustrated in Fig. 22(a) and (b) for two typical line sensors, the dark current is seen to increase rapidly with transfer-pulse amplitude on the left side of the display (detectors near the output). This type of response was common to all samples tested and, at present, we do not have a clear explanation for this behavior. However, the thermal-imaging experiments at RADC/ESE with these 25x50-element IR-CCD area sensors indicate that the uniform, dark-current generation does not limit the performance for operation at about 80 K and frame-integration time of 30 ms.**

E. CHANNEL POTENTIALS OF THE B-CCD REGISTERS AS FUNCTIONS OF THE GATE VOLTAGES

Typical channel-potential variations as a function of the gate voltage for the B-CCD registers in the TC1199 line arrays are shown in Figs. 23 and 24.

*Private communication with F. Shepherd of RADC/ESE.
**Private communication with F. Shepherd of RADC/ESE.



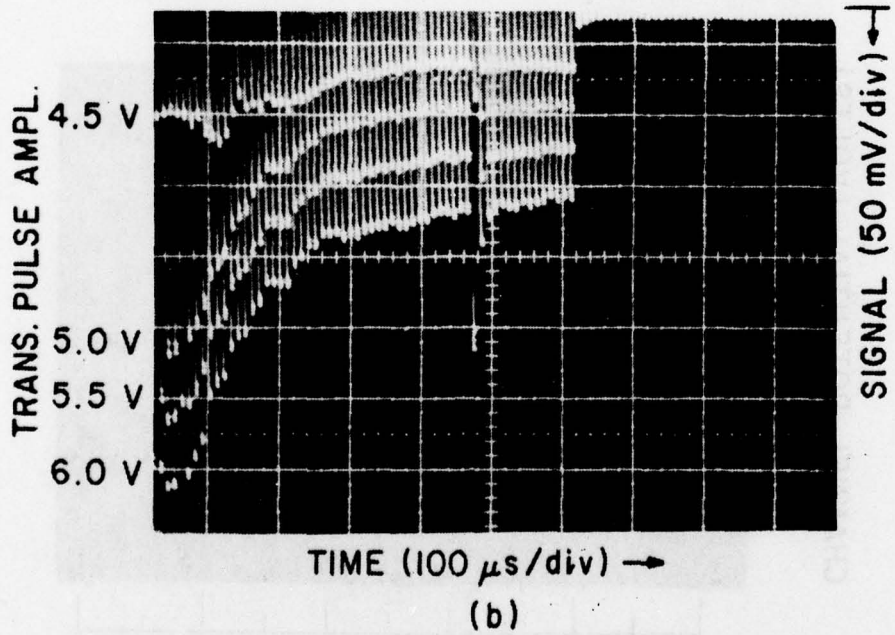


Figure 22. Dark current signatures at several transfer-pulse amplitudes for two 62-element, IR-CCD line sensors from different processing runs shown in (a) and (b) for operation at 77 K and integration time of 0.5 s.

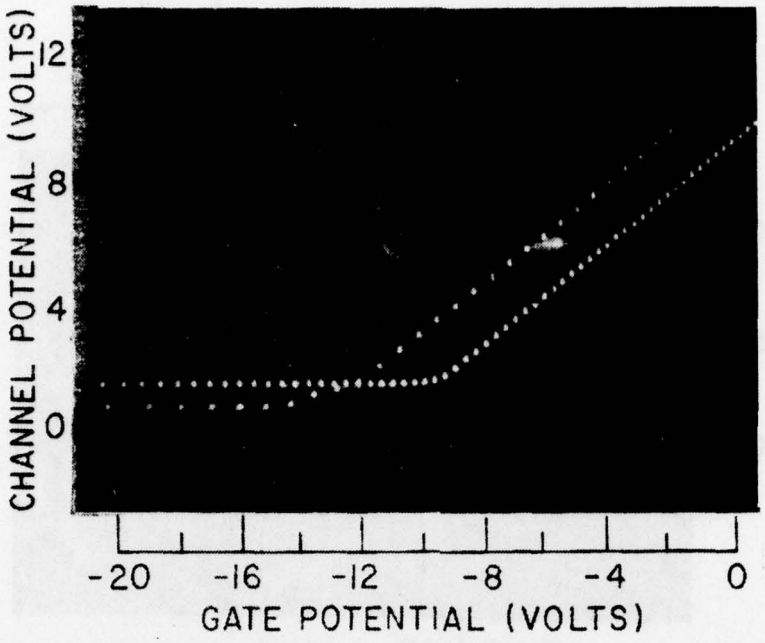


Figure 23. Channel potentials of B-CCD registers as functions of the gate voltage for the first-level polysilicon gates (the denser dots) and the second-level polysilicon gates at room temperature.

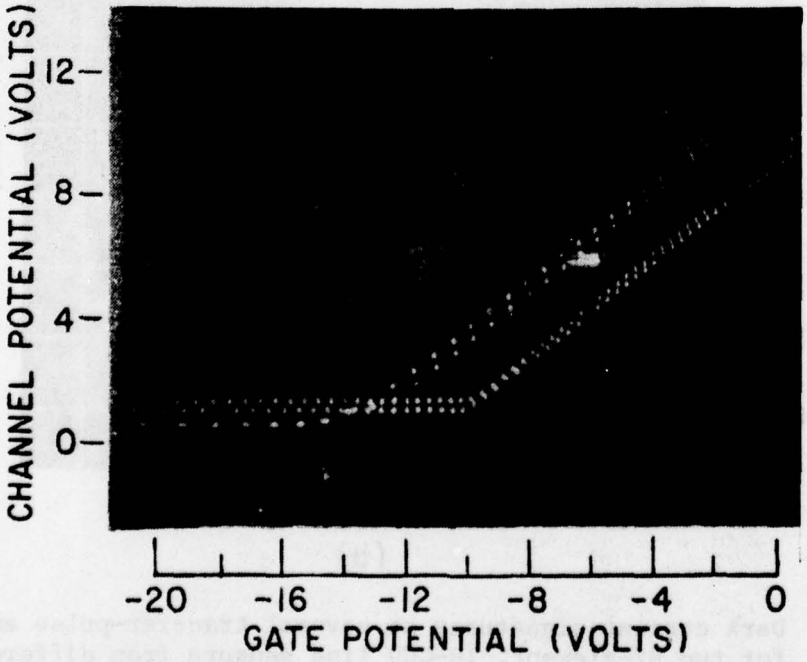


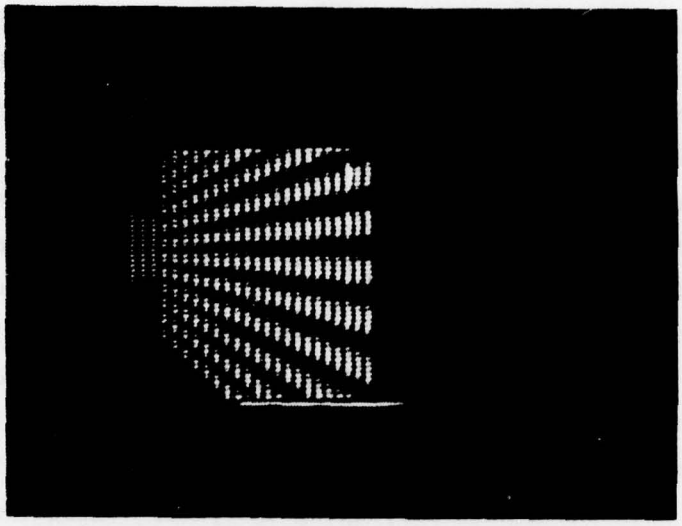
Figure 24. Channel potentials of B-CCD registers as functions of the gate voltage for the first-level polysilicon gates (the denser dots) and the second-level polysilicon gates at room temperature and at 77 K.

In Fig. 23 we show the channel potentials under the first-level and under the second-level polysilicon gates measured at room temperature. The same curves measured at room temperature and at 77 K are again shown in Fig. 24. The results in Fig. 24 point out that there is very little change in the channel potentials of our devices between the operation at room temperature and 77 K.

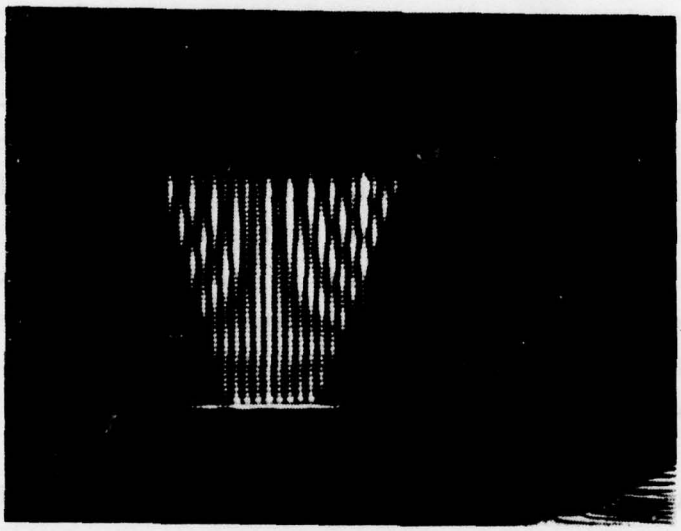
The plots of the channel potentials as functions of the gate voltages shown in Figs. 23 and 24 were obtained by turning on all of the gates along the shift register except for the one being examined. In this test, a sweep voltage lasting several seconds is applied to that gate. The drain is positively biased through a sensing circuit, while the source receives ac voltage, driving it in to and out of conduction at a 10-Hz rate. An X-Y storage oscilloscope is used with the X-axis displaying the sweep voltage from the gate under examination, the Y-axis displaying the ac signal applied to the source, and the CRT beam turned on for an instant by the drain-current sensing circuit whenever the drain current switches from off to on. Thus, the display consisted of a series of dots along the curve of minimum-channel-potential versus gate-potential. The data obtained by this method for the line-array buried-channel shift register are shown in Figs. 23 and 24. We see that even with a large negative voltage on the gate, the channels are not cut off, i.e., the channel potential is said to be "pinned" [2]. Where the possibility of complete cutoff is desired, as in the case of the transfer gate, we have used a surface channel. We also see from Figs. 24 and 25 that to get maximum channel-charge capacity, we should use negative biases on the gates, and the second-poly gates (odd-number gates in TC1199) require more negative bias than the first-poly gates (even-number gates in TC1199).

F. ROOM-TEMPERATURE STROBED IMAGING WITH THE 25x50-ELEMENT AREA SENSOR

The tests described so far do not demonstrate the imaging capability of the area arrays. It was decided not to risk the loss of area devices by immersion in liquid nitrogen, particularly since the measurements we could make with present equipment would not be quantitative, nor could we get stable images through bubbling nitrogen. We therefore chose to demonstrate operation of the area arrays at room temperature with strobed illumination. A General



(a)



(b)

Figure 25. Room-temperature, strobed operation of an area imager at a 60-Hz frame rate. (a) CRT display of a fan pattern with the higher-resolution direction going across the fan blades. (b) CRT display of a fan pattern with the lower-resolution direction going across the fan blades.

Radio strobe lamp* was triggered by the transfer-pulse logic (1199B pulser, board "A", IC package "G", pin 13, routed through pin "R" on the edge connector). The strobe lamp flashed at the frame rate, projecting a slide onto the front of the chip. The transfer gate was, of course, biased off. The image of a fan pattern is seen in Fig. 25(a) in the high-resolution direction going across the blades. The displayed image, in this case, has sufficient resolution to resolve the fan pattern. The display was on a Tektronix-602** with the deflection sweep circuits shown in Fig. 29. The video-amplifier circuit is also shown there. No video filtering was used, though a low-pass filter would have improved the picture. The image of the fan pattern rotated 90° is shown in Fig. 25(b). In this orientation, the high-resolution direction (detector spacing of 3.2 mil) is along the fan blades. The low-resolution direction (detector spacing of 6.4 mil) is across the fan. This resolution is insufficient to resolve the blades, and a moire pattern results.

*General Radio Co., West Concord, MA.
**Tektronix, Inc., Beaverton, OR.

SECTION V

TEST ELECTRONICS

A. TEST ELECTRONICS FOR THE IR-CCD AREA SENSOR

1. Waveform Generator for the IR-CCD Area Sensor

The 1199B pulser provides all the clock waveforms and bias voltages needed to operate the 25x50-element IR-CCD area sensor, as well as sweep waveforms to deflect a Tektronix-602 display. The system organization is shown in Fig. 26. The complete circuit is shown in Fig. 27, except for the display board which is shown in Fig. 28. The system is built in a small cabinet with four circuit boards.* As seen in Fig. 27, most of the components are mounted on the plug-in boards. Frequently-used controls are mounted on the front panel. There is a digital voltmeter on the front panel with a 16-position selector switch, permitting it to monitor many bias levels and pulse amplitudes. The chip holder is connected to the pulser-box through a 36-pin Amphenol connector mounted on the rear panel of the cabinet. The 28-pin dual-in-line ceramic package containing the 25x50-element area array (or its socket) is wired to the identical pin numbers on the 36-pin connector. This correspondence can be seen by comparing the function designations and pin numbers in Figs. 7 and 27. An Amphenol 14-pin connector, also on the rear panel, is used to power the box as shown in Fig. 27. The ac-operated power supply is separate from the pulser box to minimize hum on the video signal.

Board "C" contains the 555 oscillator (U-1) that generates the horizontal line rate. It gates an oscillator (U-2) that runs at four times the C-clock frequency. A pair of "D" flip-flops are driven by U-2 and cross-coupled to produce the four, double-clocked pulse trains which are buffered by U-38 to U-41, amplified by U-5 to U-8, level-shifted and applied to the four C-register gates. This board also contains the circuitry for generating the

*The equipment described in Section V has several minor changes from the equipment delivered to RADC/ESE in 1977, and described in Ref. 1, except for board "V" which is new.

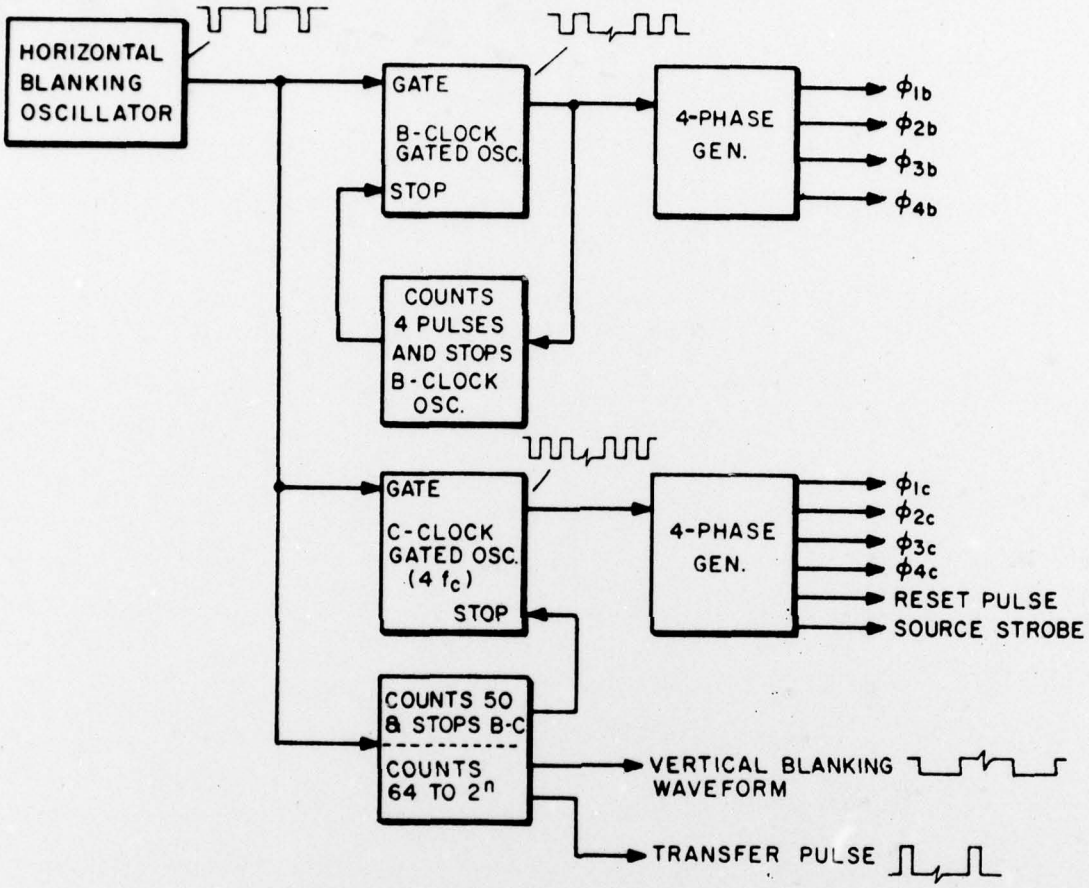


Figure 26. Block diagram of the drive circuit (subscript b refers to the the column registers; subscript c, to the output register).

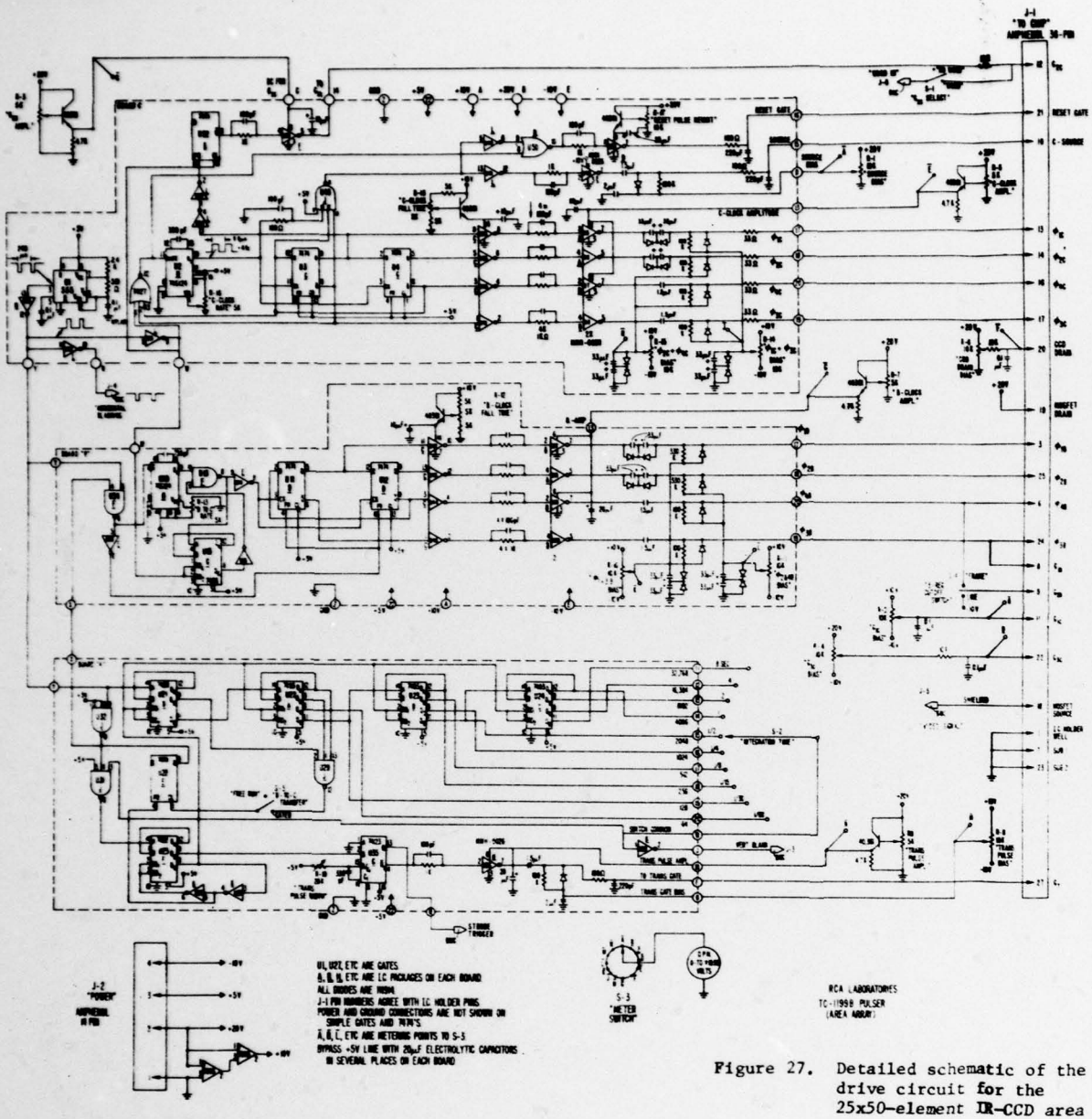


Figure 27. Detailed schematic of the drive circuit for the 25x50-element IR-CCD area array.

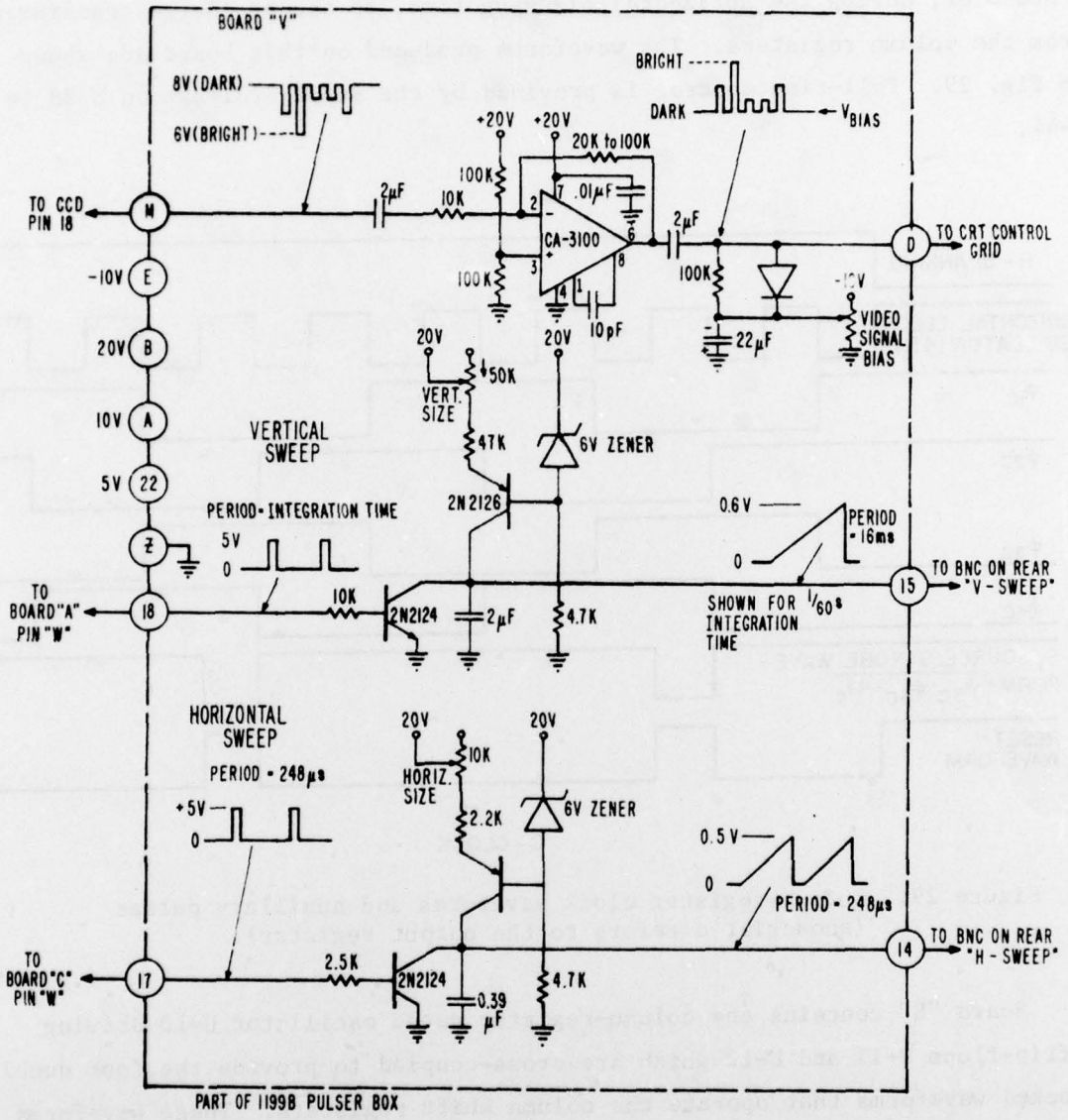


Figure 28. Detailed circuit of board "V" with the video amplifier and the horizontal and vertical sweep generators.

strobe pulses for the source-diffusion and reset pulses for the reset gate. Additional gates on this board force the clock waveforms to stop with phases 1 and 2 on, during the horizontal blanking time, to accept charge transferred from the column registers. The waveforms produced on this board are shown in Fig. 29. Fall-time control is provided by the supply voltage on U-38 to U-44.

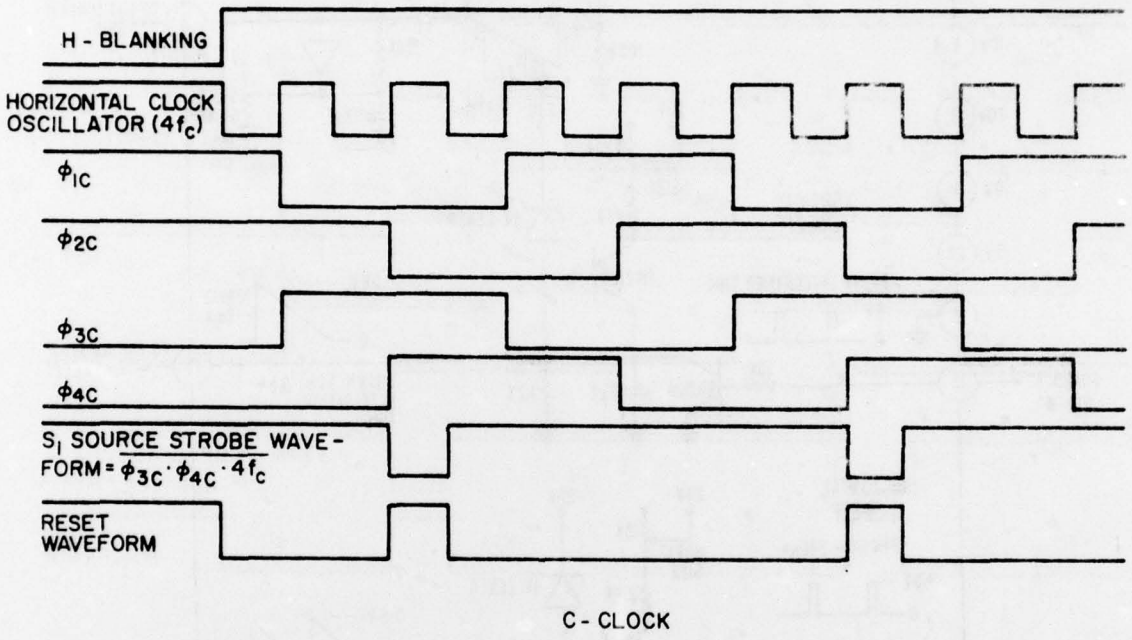


Figure 29. Output-register clock waveforms and auxiliary pulses (subscript c refers to the output register).

Board "B" contains the column-register gated oscillator U-10 driving D-flip-flops U-11 and U-12 which are cross-coupled to provide the four double-clocked waveforms that operate the column shift registers. These waveforms are buffered by U-42 to U-45, amplified by U-17 to U-20, and level-shifted by clamp circuits. The oscillator U-10 is gated from board "C" to run only during the horizontal blanking time. It is also gated by U-13 and U-15 to run only one bit for each horizontal line. The column-register waveforms are shown in Fig. 30. Fall-time control of these waveforms is provided by separately controlling the voltage supplying U-42 to U-45.

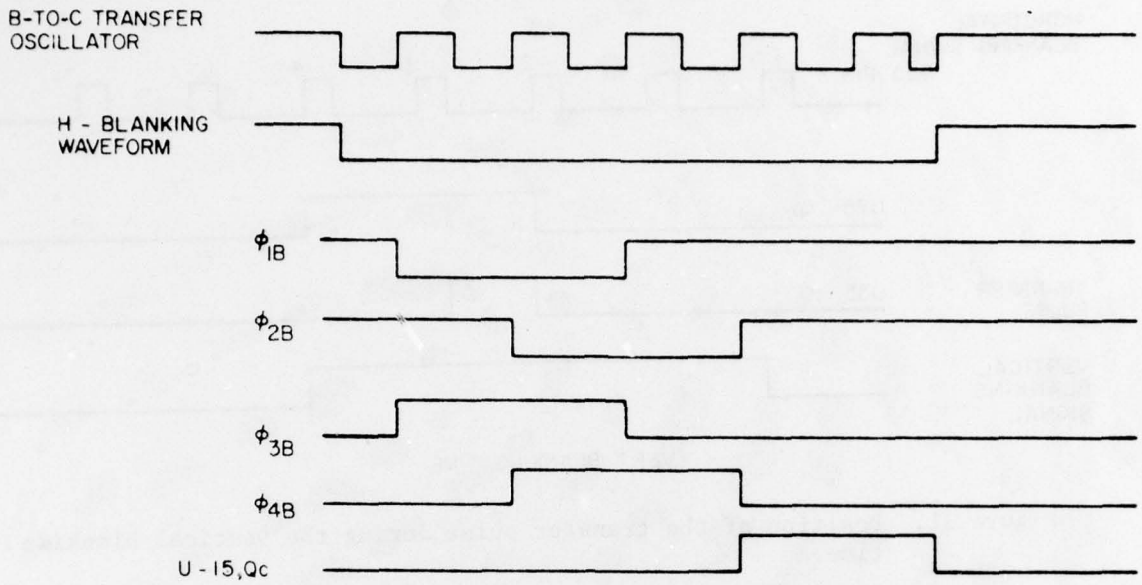


Figure 30. Column-register waveforms during column-to-outout register transfer. (subscript b refers to the column registers).

Board "A" counts the horizontal lines and generates a vertical-blanking pulse when the preset count is reached. The count can be set in binary steps from 64 to 32,768, corresponding to staring times of 1/60 s to 8 s. The vertical-blanking time lasts for four horizontal-line times and has a short transfer pulse at its center. This is shown in Fig. 31. The transfer-pulse width is set by U-35. Its height is set by U-36, and its offset by a clamp circuit. Switch S-5 determines whether the column registers advance one bit after every horizontal-blanking time or just during the first 50 after a transfer pulse.

Board "V" supplies sweep waveforms and video signal to operate the display (Fig. 28). Each of the two sweep circuits has a constant-current generator to charge a timing capacitor. Each has a transistor turned on by the logic-level blanking pulses to hold off the sweep. When the blanking pulse ends, the capacitor charges linearly. A CA-3100 IC operational amplifier inverts and amplifies the signal from the on-chip MOSFET. Its output level is shifted and applied to the control grid of the display CRT.

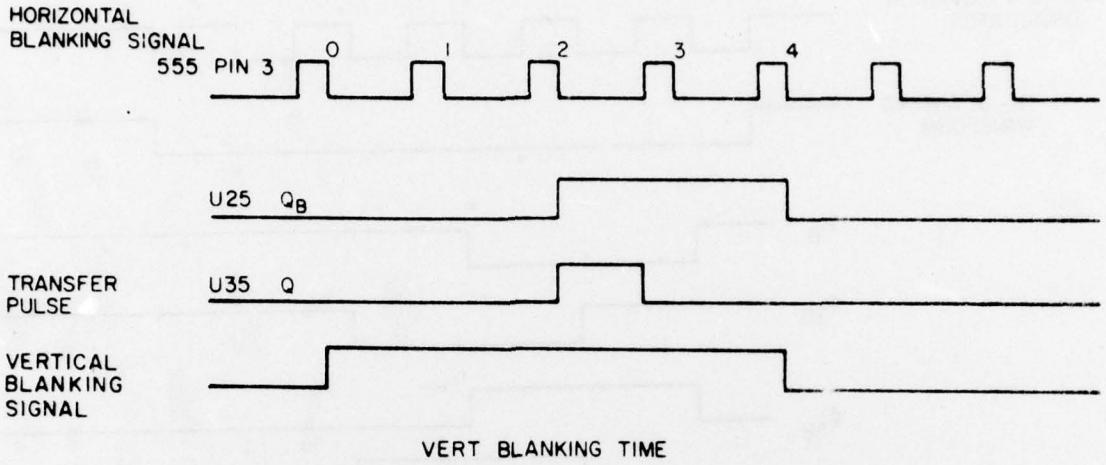


Figure 31. Position of the transfer pulse during the vertical blanking time.

2. Timing for the IR-CCD Area Sensor

The frame readout time is nominally 1/60 s. During this time interval, 68 horizontal lines are read out, made up of 64 from the divider, and 4 from the vertical-blanking-time generator. Only the first 50 horizontal lines after the vertical-blanking pulse carry any signal. When more integration time is desired, the counter on board "A" counts more horizontal lines. Thus, more time is left between vertical-blanking pulses, and hence between transfer pulses, but the time required to read out the 50-line frame remains the same. The horizontal-blank-pulse period is 245 μs; 45 μs of that is the blanking time. During the remaining 200 μs, the clock, running at 300 kHz, can read out 60 bits. The 25 charge packets from the columns are present in alternate bits for the first 50 bits. The last 10 are just overscan bits, and need not be blanked since they carry no signal.

3. Typical Operating Voltages for the IR-CCD Area Sensor

The typical operating voltages for the IR-CCD area array are shown in Table 3. The source-strobe bias and the G_{1C} and G_{2C} voltages interact, and need to be set up individually for each chip so the "typical" settings cannot be taken too seriously. The clock amplitudes in the range of 12 to 16 V gave

TABLE 3. 1199-B - TYPICAL AREA-ARRAY OPERATING VOLTAGES

	Range (volts)	Typical Setting (volts)
SOURCE STROBE BIAS	0 to 20	14.9
G_{1C}	-10 to 10	-6.3
G_{2C}*	-10 to 10	-2
G_{3C}	-10 to 10	+1.25
C-CLOCK AMPL	0 to 20	+16
DRAIN	0 to 20	+18
ϕ_{1c} & ϕ_{3c} BIAS	-10 to 10	-9
2c & 4c BIAS	-10 to 10	-2
B-CLOCK AMPL	0 to 20	+16
ϕ_{1B} & ϕ_{3B} BIAS	-10 to 10	-9
ϕ_{2B} & ϕ_{4B} BIAS	-10 to +10	-2
TRANS BIAS	-10 to +10	-2.0
TRANS PULS AMPL	0 to 20	+2 to +9

*The G_{2C} adjustment on the front panel controls a pulse amplitude in the original 1199-B box. The circuit is modified to remove the pulse, and instead apply dc from the G_{2C} pot to G_{2C}. The pot is connected from -10 to +10 V.

the best pictures in the strobed imaging tests. Higher clock amplitudes caused chip failures, particularly the B-clock. With some chips, it was necessary to vary the clock amplitudes and bias controls to converge on a satisfactory combination.

B. THE WAVEFORM GENERATOR FOR THE 62-ELEMENT IR-CCD LINE SENSOR

The circuitry for driving the 62-element IR-CCD line sensor is also built into a small cabinet with front-panel controls and a digital voltmeter for

setting up bias and amplitude levels. The complete circuits are shown in Fig. 32. Most of the components are mounted on the two plug-in boards.

The integration time is set by chip "S," a 555-oscillator whose high and low times are very asymmetric. The 555-output gates the clock oscillator, chip "I." Switch S-3 controls whether the clock oscillator runs during the long or the short interval of the 555-output. When the detectors are run in the voltage-reset mode (also known as the "vidicon" mode), it is desirable to run the clock for most of the integration time ("RUN-LONG" in Fig. 32) so that shift-register dark current is continuously run out. Of course, only the first 62-bits yield data. When the detectors are run in the continuous-skimming mode, the shift register must be stopped for most of the time. For such operation, S-3 is set ("RUN-SHORT") to run the clock oscillator for the shorter interval which is just long enough to run out the 62 bits. When S-1 is the the "WORD" position, the clock oscillator "I" does not see the integration time oscillator "S" and runs continuously for electrical input experiments. Gate A (pins 8, 9, 10 & 11) ensures that the clock oscillator stops only when the condition for detector loading is reached; namely, phases 1 and 4 on. The reset pulse is logically derived from the clock waveforms and amplified by chip "M."

All of the above circuitry is on board "B." Board "A" has the transfer-pulse-width control (chip J), the transfer-pulse amplifier (chip Q), and its level shifter. Also on board "A" is the source-strobe amplifier (chip "P") and its level shifter. Logic for the source strobe comes from board "B." The timing of the clock, the source strobe, the reset, and the transfer waveforms are shown in Fig. 33. As in the area-array pulser box, a 36-pin Amphenol connector is mounted on the rear panel for direct connection to the chip with identical pin numbers. This correspondence can be seen by comparing the schematic of the test electronics in Fig. 32 with the schematic of the chip in Fig. 13. A 14-pin Amphenol connector is provided for power as in the area-array electronics.

Typical operating voltages for the line sensor are shown in Table 4. The same comments discussed above for the area sensor apply. The values in this table were for 77-K operation, but no consistent difference was seen at room temperature.

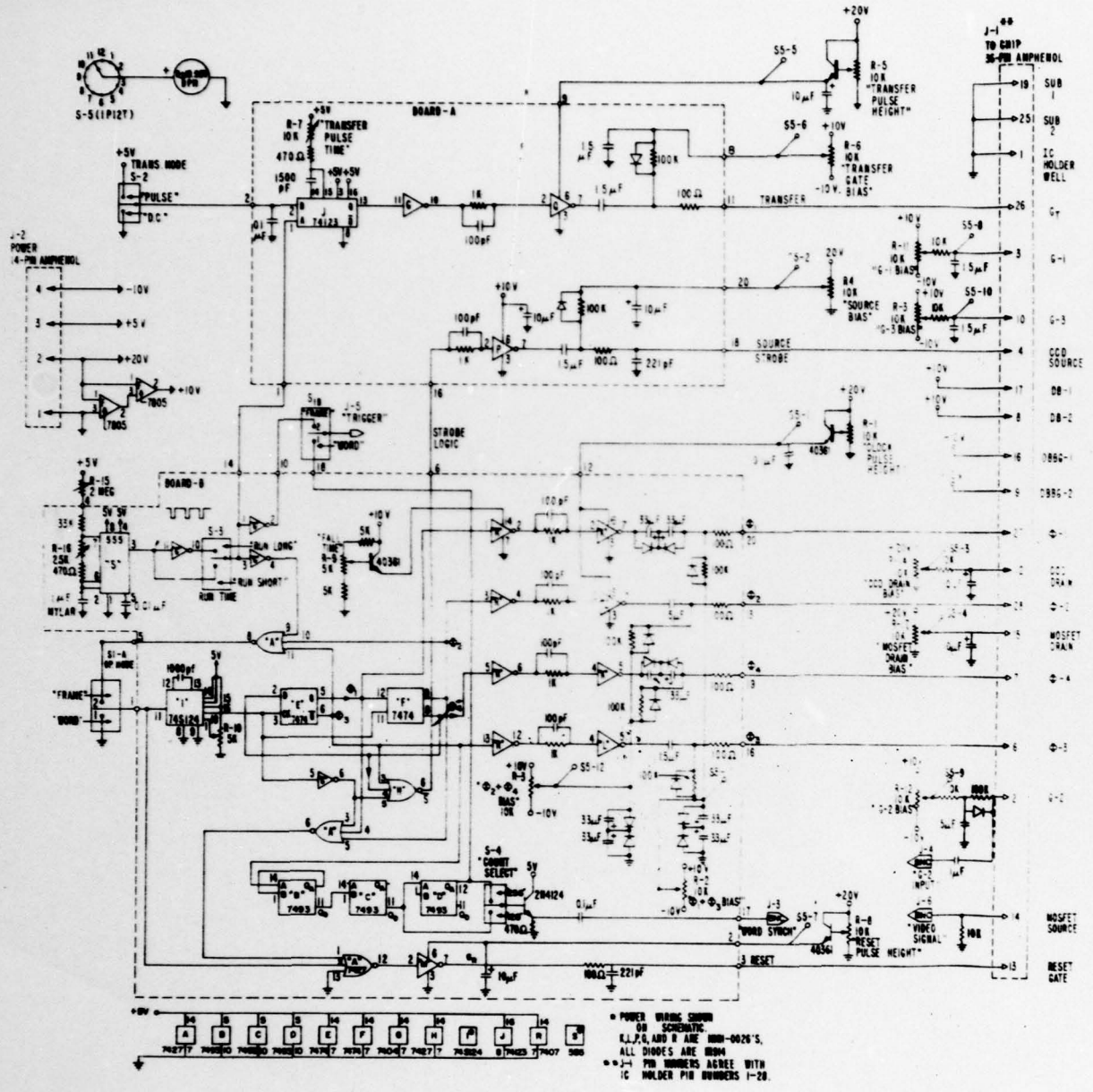


Figure 32. Detailed schematic of the drive electronics for the 62-element line sensor.

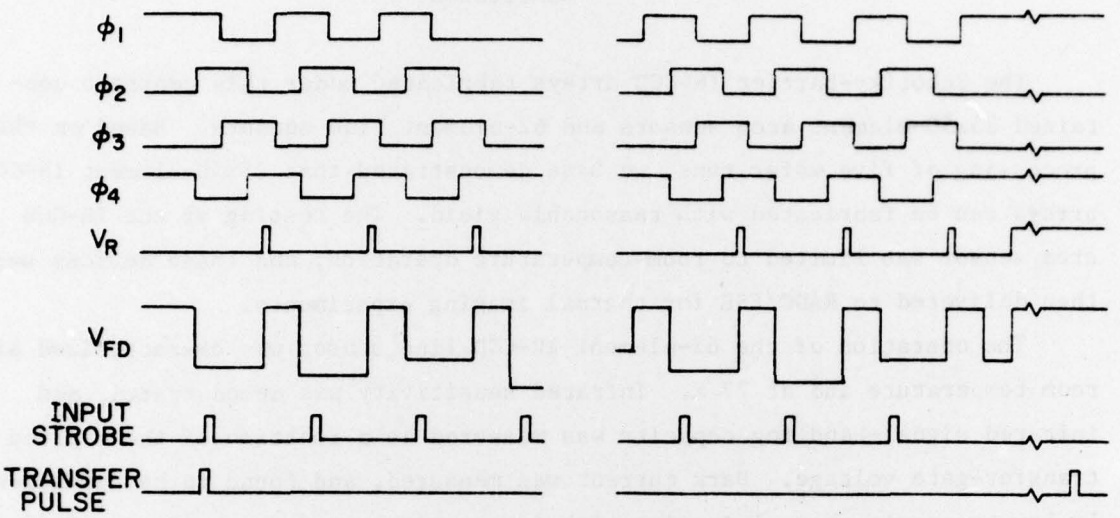


Figure 33. Pulse timing for the 62-element line sensor.

TABLE 4. 1199-A - TYPICAL LINE-ARRAY OPERATING VOLTAGES

	Control Range (volts)	Typical Setting (volts)
Clock Pulse Height	0-20	10-16
Source Bias	0-20	11.6
CCD Drain Bias	0-20	15.3
MOSFET Drain Bias	0-20	20
Trans Pulse Height	0-20	2-10
Trans Pulse Bias	-10 to +10	-2
Reset Pulse Height	0-20	+15
G_1 Bias	-10 to 10	-4
G_2 Bias	-10 to 10	-4.5
G_3 Bias	-10 to +10	-2.1
$\phi_{1\&3}$ Bias	-10 to +10	-10
$\phi_{2\&4}$ Bias	-10 to +10	-3.6

SECTION VI

CONCLUSION

The Schottky-barrier IR-CCD arrays fabricated under this contract contained 25x50-element area sensors and 62-element line sensors. Based on the processing of five wafer runs, we have demonstrated that 25x50-element IR-CCD arrays can be fabricated with reasonable yield. The testing of the IR-CCD area sensor was limited to room-temperature operation, and these devices were then delivered to RADC/ESE for thermal imaging experiments.

The operation of the 62-element IR-CCD line sensor was characterized at room temperature and at 77 K. Infrared sensitivity was demonstrated, and infrared signal-handling capacity was measured as a function of the applied transfer-gate voltage. Dark current was measured, and found to be sufficiently low to permit thermal imaging with integration times in the range of 30 to 100 ms. Room-temperature imaging was demonstrated with the 25x50-element area sensors, indicating good shift-register operation.

The process modifications studied under this program were made to optimize the detectors, to protect the back surface, and to improve yield. The processing parameter most extensively studied was the formation of the platinum silicide which was done by a high-temperature sintering at 650°C, and a low-temperature sintering at 320°C.

The thermal-imaging measurements made at RADC/ESE with the 25x50-element IR-CCD area sensors demonstrated temperature resolution of about 1°C for frame integration times of 30 ms. Comparable performance was achieved for the area sensors with the platinum silicide detectors sintered at the high and the low temperature.

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